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FROM THE DESK OF
EXECUTIVE EDITOR...

Dear Readers,

The qualitative and timely publication of Vol. V / Issue II(Jul-Dec 2015) of our esteemed International Journal of Engineering, Sciences and Management (ISSN: 2231-3273) has brought great joy and happiness to the entire fraternity of the journal and honorable members of the Editorial and Advisory Board. The board members rich experience and varied expertize is providing immense succour in propelling the journal to attain an envious position in areas of research and development and accentuate its visibility. The distinctive feature is indexing of the journal by Jour Informatics, Index Copernicus, Google Scholar and DOAJ. It is a matter of great pride and honor that the journal has been viewed by researchers from one hundred and twelve countries across the globe.The aim of journal is to percolate knowledge in various research fields and elevate high end research.The objective is being pursued vigorously by providing the necessary eco-system for research and development.

Large number of research papers were received from all over the globe for publication and we thank each one of the authors personally for soliciting the journal. We also extend our heartfelt thanks to the reviewers and members of the editorial board who so carefully perused the papers and carried out justified evaluation. Based on their evaluation, we could accept fourteen research papers for this issue across the disciplines. We are certain that these papers will provide qualitative information and thoughtful ideas to our accomplished readers. We thank all the readers profusely who conveyed their appreciation on the quality and content of the journal and expressed their best wishes for future issues. We convey our deep gratitude to the Editorial Board, Advisory Board and all office bearers who have made possible the publication of this journal in the planned time frame.

We invite all the authors and their professional colleagues to submit their research papers for consideration for publication in our forthcoming issue i.e. Vol.VI| Issue I|Jan-Jun 2016 as per the "Scope and Guidelines to Authors" given at the end of this issue. Any comments and observations for the improvement of the journal are most welcome.

We wish all readers meaningful and quality time while going through the journal.

Wg Cdr (Prof) TPN Singh
Executive Editor
International journal of Engineering, Sciences and Management (IJESM)
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July 2015

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A STUDY ON HARDWARE TROJAN DETECTION AND TAXONOMY

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ABSTRACT

Hardware Trojan (HT) is a malicious modification of the circuitry of an integrated circuit. Hardware Trojan is completely characterized by its physical representation and its behavior. Thus there should be some means of Trojan detection and timely elimination of such threats in the designed circuitry. Through this research, we analyzed detail taxonomy of Trojans. Then perform side channel analysis on the performance of the designed system before and after introduction of Trojans in the programming logic embedded in the Integrated circuit. Then the degree of corruption will be analyzed by comparing the bandwidth of side channel of the signals obtained before and after introduction of Trojans. Also protocols will be defined to eliminate such introduced Trojans and to define methods to recover from potential Trojan attacks. Also a case study about Trojan attacks in fiber optic system and its effects will be discussed in the paper.

Keywords- *Bandwidth, embedded, elimination, fiber optic system, integrated circuit, protocols, side channel analysis.*

1. INTRODUCTION

In today's era, digital systems are an integral part of almost all relevant mechanisms and phenomena driving them. Thus with the increase in reliance on digital systems, their security remains an issue of utmost importance. There could be a breach in the security and performance of these systems and indirectly their performance through myriad of ways. Even the smallest of a bug in such small systems could lead to catastrophic results of system performance and the outcomes, subsequently following them. As per a recent FBI report***, "the net loss due to such attacks in the last decade was estimated up to $22.5 billion"***. Thus there should be effective counter measures to identify such attacks and understand the behavior or patterns of such attacks. One such way could be definition of protocols. This will help system designers and developers around the globe to mitigate any future threats evolving on such systems.

Thus keeping an insight of the discussed points in the last paragraph, this research manuscript is divided into following 5 sections that will demonstrate effective ways of digital and hardware system security from Trojans:

Section 1 discusses the literature survey on Trojan Taxonomy and detection

Section 2 explains Practical hardware architecture implementation and effects of Trojan attacks

Section 3 gives information about Performance evaluation of the system under test

Section 4 defines the protocols for Trojan Detection

\We conclude different techniques to detect Trojans and future scope of the research in Section 5.

2. LITERATURE SURVEY ON TROJAN CLASSIFICATION/TAXONOMY AND TROJAN DETECTION TROJAN TAXONOMY

Trojans can be classified into three principle categories as shown in the Figure below, i.e., according to their physical, activation and action characteristics.

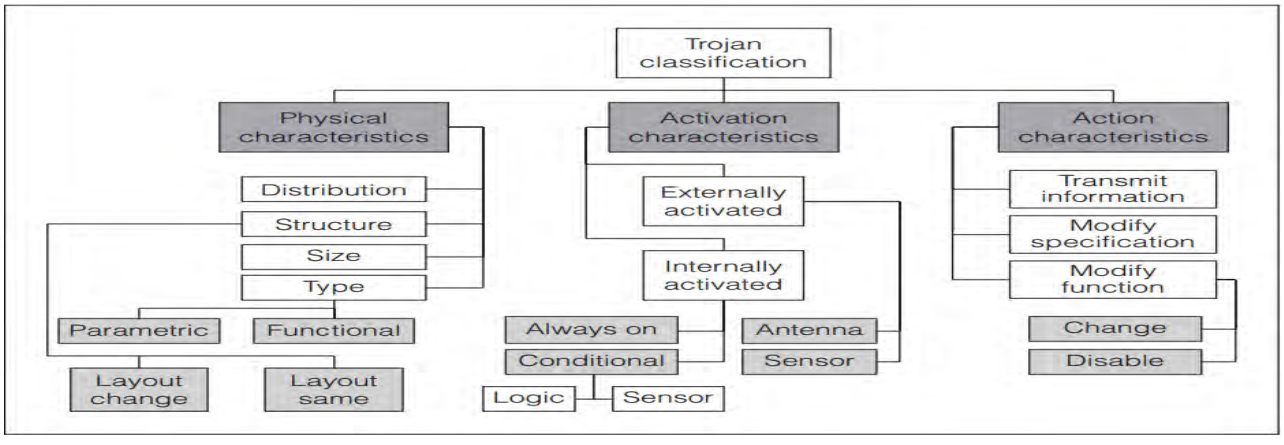

Fig.1. A Classification of Trojans

Let us understand the classification shown above:

1. PHYSICAL CHARACTERISTICS: The physical characteristics category describes the various hardware appearance of Trojans. This type of category divides Trojans into *functional* and *parametric classes*. The functional class involves Trojans that are manually imbibed by addition or subtraction of transistors or gates or their *scaling effects*. Whereas the parametric class extends to the Trojans that are completed by adjustments of parasitic of a circuit such as current wires and logics. The size subclass is the number of elements in the chip that are brought, deleted or settled. The distribution subdivision depicts the placement of the Trojan in the chip's layout. The structure subclass mentions to the face when an opposition is pushed to animate the setup to introduce a Trojan, which can cause the physical layout of the chip to change. These type of changes can lead to different location for some or all planned elements. Any bad alterations in the material plan by Trojans could alter the chips functionality and power features.

2. ACTIVATION CHARACTERISTICS: Activation characteristics is the base for comparison that causes Trojan to get activated and start its routine function. Trojan activation characteristics are divided into two classes which are: *externally activated* (e.g., an antenna or a sensor for interaction with the outer space) and *internally activated* (further classified as always on and condition based), as ‘‘Always on’’ means that the Trojan is always in active state and the Trojan can damage the on chip functionality at any time. This type of subdivision includes Trojans that modifies the chips dimensions in such a way that certain nodes and paths face failure easily. The opposition can use nodes or paths to insert Trojans that are rarely used. The condition based subdivision has Trojans that aren’t active until a particular discipline is met. The activation condition is based on the outcome of a sensor that supervises temperature, voltage, or any type of external environmental condition (such as electromagnetic, disturbance, humidness, height, or physical property).

3. ACTION CHARACTERISTICS: Action characteristics identify the types of insubordination behavior introduced by the Trojan. The action characteristics is divided into three categories: *modify function*, *modify specification*, and *transmit information*. The modify function are the Trojans that alters the chips performance by adding or removing logic or avoid current logic. The modify-specification class refers to Trojans that focus their attack on changing the chip’s parametric properties, like scaling of devices when an opposition alters living wires and transistors connections. Eventually, the transmit-information subdivision lets in Trojans that carry important information to an opposition. Researchers have designed many types of Trojans to evaluate their detection techniques by targeting them and understanding their behavior under different test and features.

TROJAN DETECTION

After classifying Trojans we define various techniques to detect them based on their behavior, once they enter into the circuit or the on chip or processor software architecture. The various methods of detection are as follows:

1. Side Channel Signals Analysis: This is a type of attack which gathers information from physical execution of a cryptosystem, than the theoretical part of an algorithm. There are different techniques in which a system can crack, for instance power intake, timing data, EM leakage, all these examples will give extra data to the device. Internal operations

can be done if we have the technological information of the system. Statistical power analysis is used in lots of side channel analysis. Side-channel analysis attacks are not the attacks if efforts are being made to crack a cryptosystem by unlawful methods. There are many types of side channel analysis which include timing attack, power-monitoring attack, EM attacks and many more. In timing attack, the information which is sent in and out of the CPU is being monitored on a device. We can get the secret key by just watching the time it takes to perform cryptographic operations. These type of attacks also uses statistical analysis. In power analysis attack, an attacker just observes the power intake of the device and eventually attacks it. These attacks can be reduced if we reduce the leakage of data and also by canceling the bonding between data information and secret data. Thus with this information on side channel analysis a Trojan could be detected , for instance by comparing the bandwidth of the signal with and without Trojan, by means of a spectro meter.

2. Automatic Test Pattern Generation: in this type of method we need to find the difference between the right circuit and the defected circuits stimulated by flaws. These differences can be found out by just sending an input signal to a digital circuit which activates automatic test tools. The patterns which are generated are taken to test the devices after they are produced. The strength of ATPG is calculated by the quantity of defects, or faults. The ATPG should also have a very good efficiency. Basically, a fault is caused when a device is being manufactured. The outputs of the test patterns can be known by the measurements detected at the systems first outcome when we apply the test patterns to any device. The expected output is a kind of output which can be found out from the output of the test pattern when we examine a defected-free device. There are two types of fault models, which are single fault and multiple fault models. In a single fault model only single fault can be detected in a device, whereas in multiple fault models there are many defects which can be detected. Now, there are many faults under these two type of faults. The fault collapsing technique is when there are more than two faults having same defect behavior for all incoming patterns. Next, the stuck-at fault model, this is the most widely practiced model used in past several years. In this type of fault model it is considered that a signal is stuck at a certain value in a circuit. Other type of fault is transistor faults, these types of faults are used to explain the defects in CMOS gates. And lastly the bridging fault, when two signals are being short circuited then these type of defects occur.

3. Failure Analysis-based Techniques*:* in this type of technique we are gathering all the information and finding out what caused the systems failure. This is a very important process in many departments of Production Company, like an electrical company where it is used to as vital equipment for a better product. The failure analysis technique depends upon the failed devices for analyzing the cause of failure. There are many ways by which a device can be analyzed, which are microscopes, sample preparation, radiography, spectroscopic analysis and many more. In microscopes there are many types of microscopes which are used for analyzing purpose, which are optical microscope, scanning acoustic microscope, x-ray microscope etc. sample preparation technique uses plasma etcher, back side thinning tool to prepare a sample for analyzing. In radiography we analyze the defected devices by neutron radiography and x-ray radiography.

3. HARDWARE IMPLEMENTATION

Through this research, after understanding the taxonomy and methods of detection of Trojans, let us now look at the practical demonstration of the effects of these Trojans when they get introduced in a system or a circuit.

We have practical implemented a model for the effects of Trojans using the Beaglebone Black Development board. The specifications of the board are as follows:

Parameter	Feature
On board Processors	AM3358 1GHz ARM Cortex-A8 processor TI AM3358 Sitara™ Processor
Pipelining architecture	Dual pipelining
Architecture	Reduced instruction set Computing(RISC)
Operating systems supported	*ARM compatible linux 3.8 kernel, debian, android, Uuntu, angstrom*
cache	Level-1: cache division for rules and information Level-2: unified cache

Table 1) Specifications of Beaglebone Black Board

Now let us consider the on board LED of the Beagle black board is used to transmit signals or used as a source of excitation for a fiber optic cable. The operation of board under normal conditions is shown in the figure below.

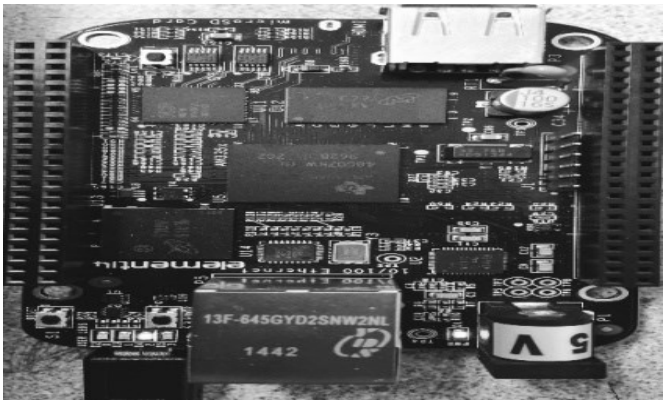

Fig. 2. Beagle Board Black used for Fiber optic cable excitation

Under the normal operating conditions of the beagle black board we can see that 2 LED's are glowing, which are USR0 and USR2. The USR0 will blink in the heartbeat pattern and USR2 will show us the CPU activity of the board. The USR0 is used for signal transmission over the proposed optical fiber network. This is the normal working condition of the board. Thus the desired signal will get transmitted as it is.

```
tick = setrange(togLED, 10);/tick will set the toggle rate of the LED PATTERN GLOW
stoptick= function() {/function to implement blink
clearInterval(tick);
};setTimeout(stopTick, 3000);/set tick freq.
```

The above is the source code used for transmission of signal over the Fiber optic system.

Now if we consider the system/circuit is connected for routine maintenance or scheduling to a computer or a remote server, for system upgradation purposes. If by chance a Trojan gets introduced, it may cause serious implication in the functioning of the circuit. The figure below shows the effect on beagle board when the Trojan is introduced.

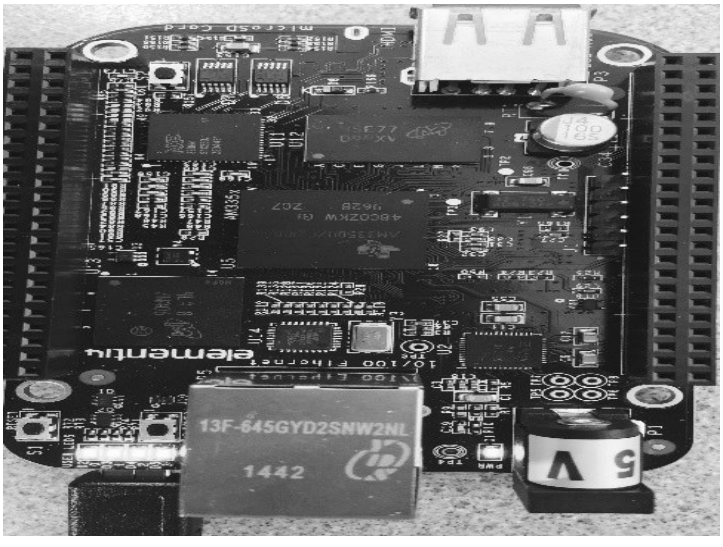

Fig. 3. Activity of LED on board after introduction of Trojans

From the figure we can see that, all the LED's will start glowing at the same time. This will thus transmit an inappropriate signal at the receiving end.

On further analysis it was found that such an implication took place, because the Trojan changed the delay sequence in the LED blinking sequence as shown below

```
tick = setrange(togLED, 100);/tick will set the toggle rate of the LED PATTERN GLOW
stoptick= function() {/function to implement blink
clearInterval(tick);
};setTimeout(stopTick, 3000);/set tick freq.
```

As shown in the routine above the Trojan introduced changed the toggle to 100 from 10 thus causing the pattern to change.

4. SIDE CHANNEL ANALYSIS OF TROJAN DETECTION

As discussed earlier in the manuscript a side channel analysis of the circuit tested was done. The figure below shows us the side channel analysis of the circuit without implementation of Trojans. The analysis was done by help of Tektronix spectrum analyzer.

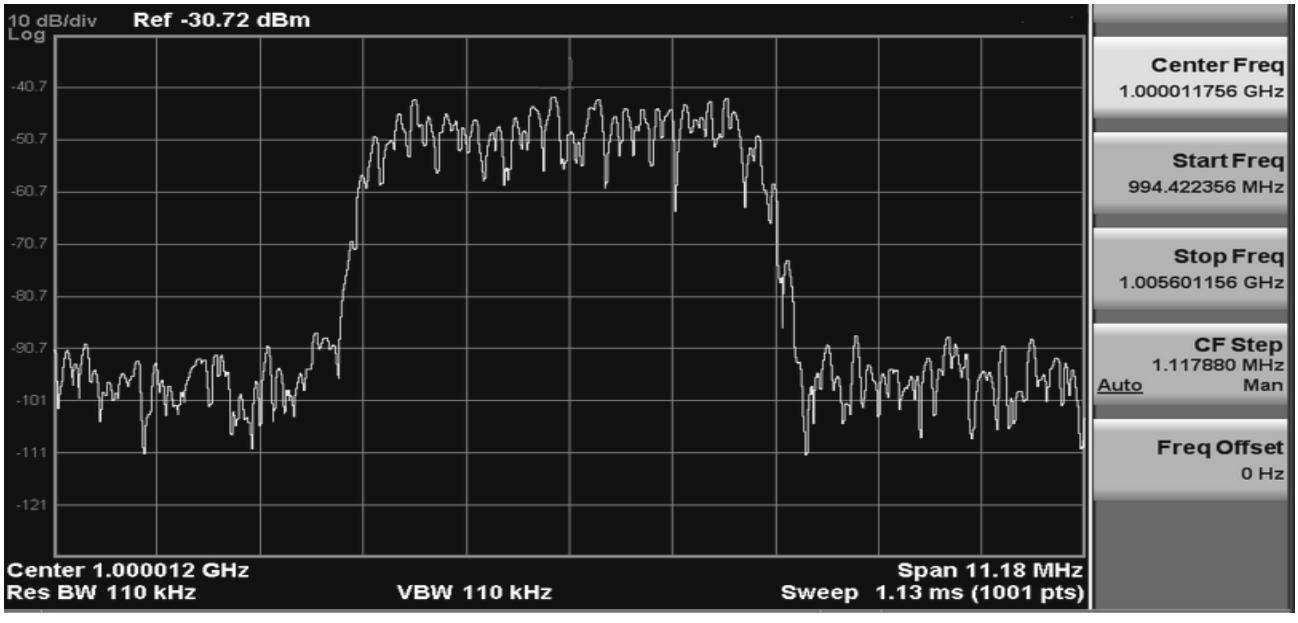

Fig. 4. Side channel analysis

Thus from the above figure we can see the bandwidth obtained during normal functioning was 110KHZ. As soon as we applied the Trojan implication code the bandwidth fell to 80KHZ and a random noise pattern was seen in the above waveform. Thus this indicated presence of Trojans and also indicated the signal corruption due to Trojan introduction.

5. PROTOCOLS TO PREVENT TROJAN ATTACKS

This section discusses the various ways by which we can prevent the attack of Trojans or detect them before they are implemented in the circuit.

PROTOCOL 1: SECURE HARDWARE CHECK As shown in the figure below we can implent a secure pair of hardware system device. Thus as shown below when the circuit is connected to a known hardware of known IP adress, then only data transfer will take place between the two devices,for the mentioned address. If the IP adress is different, it will terminate the connection immediately thus preventing the import of potential trojans from the new unpaired device.

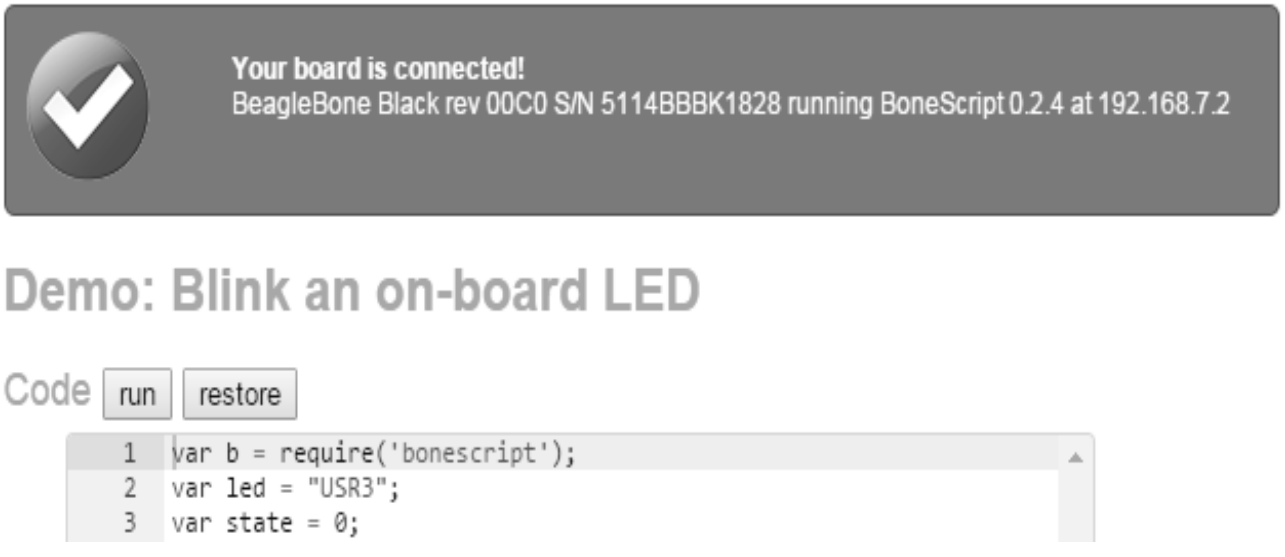

Fig. 5. Protocol 1 application: Beaglebone board connected to User PC

PROTOCOL 2: PACKET TRACING We implemented this on a client server application called Putty that enabled us to trace the packets of data that were sent over the network. Thus any loss of packet was indicated by putty. If a packet is lost, then this indicates introduction of a Trojan. Thus the user beforehand could take necessary actions to prevent attack of Trojan's on a system.

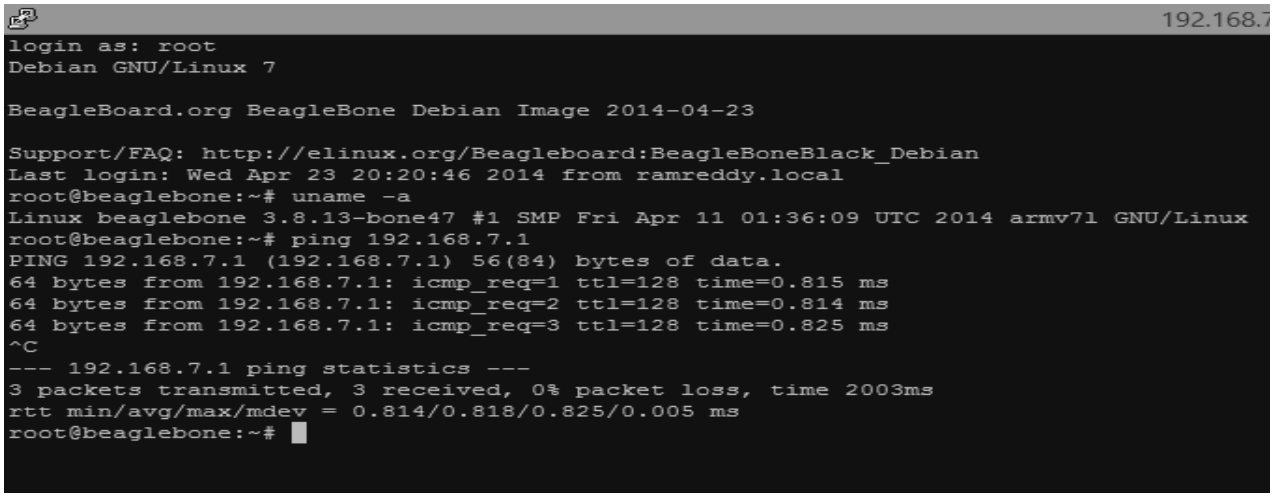

Fig. 6. Sample putty implementation on beagle board black

Once the port gets connected, then we can check login protocols to prevent unauthorized access either. The port number will automatically change depending on the log in protocol that you select from the available list. In the end, click open the button at bottom of the window and Putty connects you to the private network of the hardware component that we created earlier. We can use SSH protocol to protect from network attack called spoofing. This spoofing process secretly redirects you to another computer thus by making you send passwords to a wrong machine. In this implementation we create a virtual network of the hardware component that we connect to the system and transfer the data packets between the newly created and existing networks A security feature is added to abort the network connection if the user continuously enters the wrong password for more than 5 times so as to prevent unauthorized access to the network. When you run putty, a dialog box will appear through which you can control over the connections. Usually we don't need to change configuration options in most of the cases. But we have to give some basic parameters like host name, port number and connection type etc. The following are the steps to configure putty to make it work like a client server model.

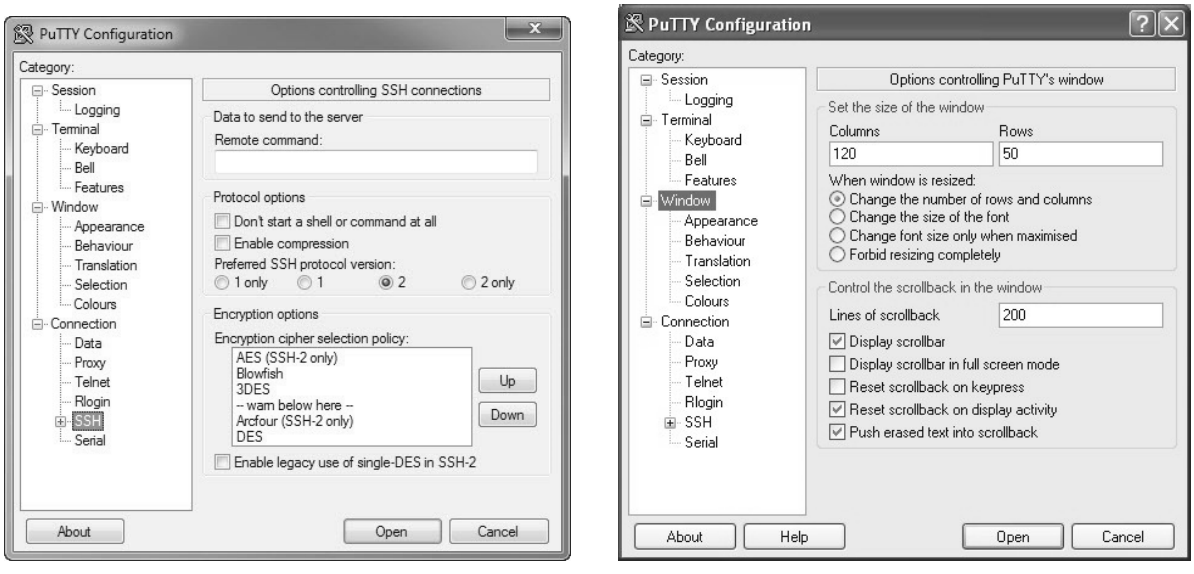

Fig. 7. Client Server Model in putty

The data packets are sent from one network to another in a timely manner. Depending upon the number of packets that are being received, loss % of the packets is calculated.

PROTOCOL 3: HARDWARE INDICATORS For this protocol implementation we used MSP430 Launchpad TI kit. It is basically a microcontroller used by beginners for microcontroller-based application. This type of microcontroller can be used to program any other type of MSP430 device. There are many types of MSP430 launch pads which includes a USB Launchpad, FRAM Launchpad and a 32-bit processor Launchpad.

When we connect this circuit to any of the portable device for any reason such as maintenance or circuit upgradation or importing additional functionality within a circuit processor we can see that the power LED starts glowing which shows that the circuit is working perfectly.

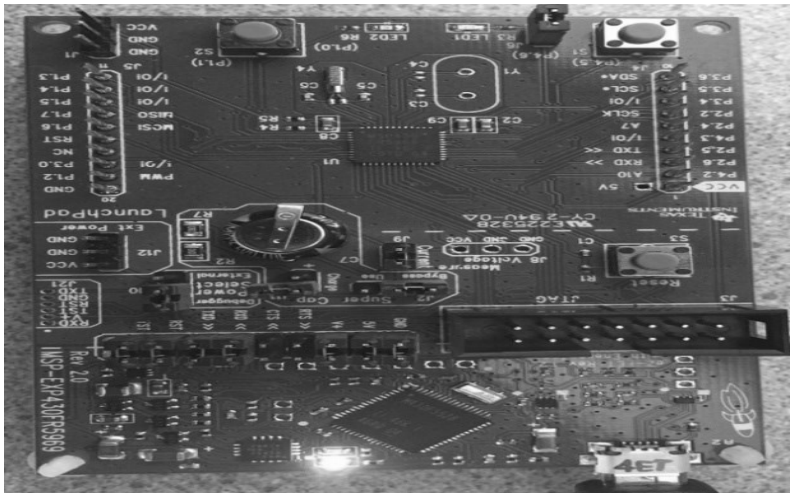

Fig. 8. Normal functioning of the circuit

If a Trojan is included in the device, by connecting it to an external device, an red LED will glow indicating inclusion of Trojans. Thus the circuit will immediately terminate from the connected device. As shown below.

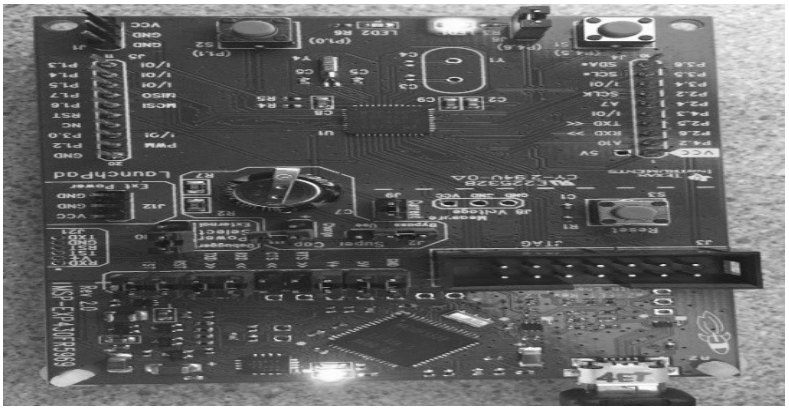

Fig. 9. Trojan introduction in the circuit

6. CONCLUSION

Through this research we were successfully able to classify Trojans and studied different techniques to detect them. Also through the hardware implementation on various development boards we were able to demonstrate the presence of Trojans and their effects. Also by side channel analysis and bandwidth monitoring we were able to see the effect of Trojans in the circuitry. In the future research, additional circuitry and chips can be installed on the board for removing the Trojan that is detected and identified.

7. ACKNOWLEDGEMENTS

Through this manuscript we like to thank Dr. Choi for giving us a chance to implement the research and also providing constant motivation and help whenever required, enabling us to learn the subject in depth.

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CACHE MEMORY ANALYSIS AND OPTIMIZATION TECHNIQUES

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ABSTRACT

Recently, it has been exceptionally vital to decrease the access read and write time from main memory and lot of study and exploration is done worldwide to lower this access time. Utilization of a small and rapid cache memory to decrease the access time has been successful and implemented in most of the system architectures. However, there has been always a tradeoff between cache memory size, memory access time, memory access speed and cost of memory. For the software to perform significantly with a high speed; a utilization of cache memory in the architecture platform can be made elegantly by using some protocols and algorithms in software programming. This paper mainly discusses about analyzing and examining the localities to accomplish maximum hit rate and reduce the overall access time by using such programming protocols and algorithms.

Keywords – *CPU Speed, Data Optimization, Hit Rate, Miss Rate, Programming Protocols*

1. INTRODUCTION

To relieve the impact of the increasing gap between CPU speed and main memory execution performance, today's computer architectures implement various leveled memory structures. The thought behind this methodology is to hide the both low main memory bandwidth and the main memory access time which is slower rather than the execution of the CPUs. Traditional single core processors had a committed caching model while the late multi-core processors have a shared cache model. But an effect of offering and increment in the number of cache levels, the cache access time increases and has a tendency to consume a higher rate of memory access time which overall influences the execution time [1]. Usually, there is very small but expensive, rapid memory placed on top of the level which is normally incorporated inside the processor chip to give data with low latency and high transfer speed; i.e., the CPU registers [2].

Moving further far from the CPU, the layers of memory progressively get to be larger and slower. The memory parts which are situated between the processor core and fundamental memory are called cache memories or simply caches. They are expected to contain duplicates of fundamental memory blocks to accelerate access to often required data [2].

The next successive lower level of the memory hierarchy system is the fundamental memory or main memory which is huge additionally relatively slow. While external memory, for example, hard disk or remote memory segments distributed data computation represents the lower end of any memory design, this paper concentrates on enhancement and

optimization techniques for improving cache performance and software programming protocols to utilize this cache to the maximum.

The levels of the memory chain of usually subset each other with the goal that information or data inside a smaller memory are also additionally put away inside the larger memories. A regular memory progression is demonstrated in Figure 1. Efficient and effective program execution must be normal if the codes regard the various leveled memory design structure. Unfortunately, today's compilers can't present profoundly complex cache based changes and, thus, quite a bit of this improvement exertion is left to the software developer [4].

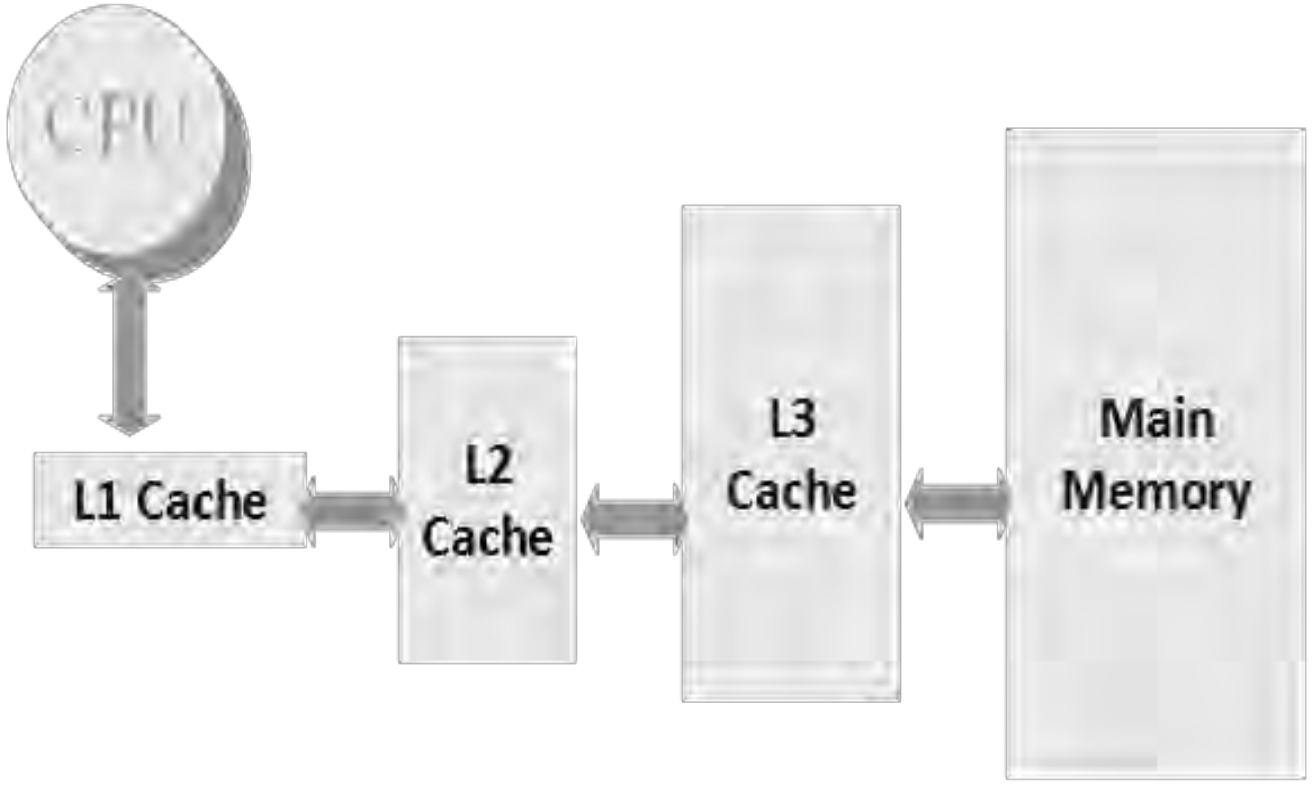

Fig. 1.Cache Memory Organization

This is especially valid for high computational, numerically concentrated programs, which our paper focuses on. Such programs occur in all science and designing controls and fields like finance software, automotive and control systems. They are characterized both by numerical operations and in addition by the way that the majority of their execution time is spent in computational pieces in view of loops and iterations. Along these lines, the fundamental data sets are ordinarily too large to be kept in a cache. To consider those issues at high level, efficient codes in scientific computing must necessarily combine both computationally optimal algorithms and memory hierarchy optimizations [4].

In Section 2, we present background study for fundamental architecture of cache memory including cache organization, cache mapping, locality of reference, processor Cache information. In Section 3, we measure and simulate the cache behavior using simple programs and performance evaluation of caches i.e. analysis. Section 4 consists of simple techniques to improve cache efficiency and general description of elementary cache optimization techniques. In Section 5, we discuss how such methods can be utilized to create cache aware algorithms and Section 6 concludes the paper.

2. FUNDAMENTAL ARCHITECTURE OF CACHE

2.1 Organization of Cache Memories Ordinarily, a memory hierarchy contains fairly small number of registers on the chip which are accessible with a greater speed. Besides, a small cache normally called level one (L1) cache is set on the chip to guarantee low latency and high data transfer capacity .i.e. high bandwidth. The L1 cache is regularly divided into two different parts; one just keeps data, the other instructions. The latency of on-chip caches is usually maybe a couple cycles [8].

As the large on-chip caches of new microprocessors running at high clock rates cannot deliver data within one cycle since the signal delays are too long. Hence, the on-chip L1 cache size is constrained to 64 Kbyte or even less for some chip designs [21].

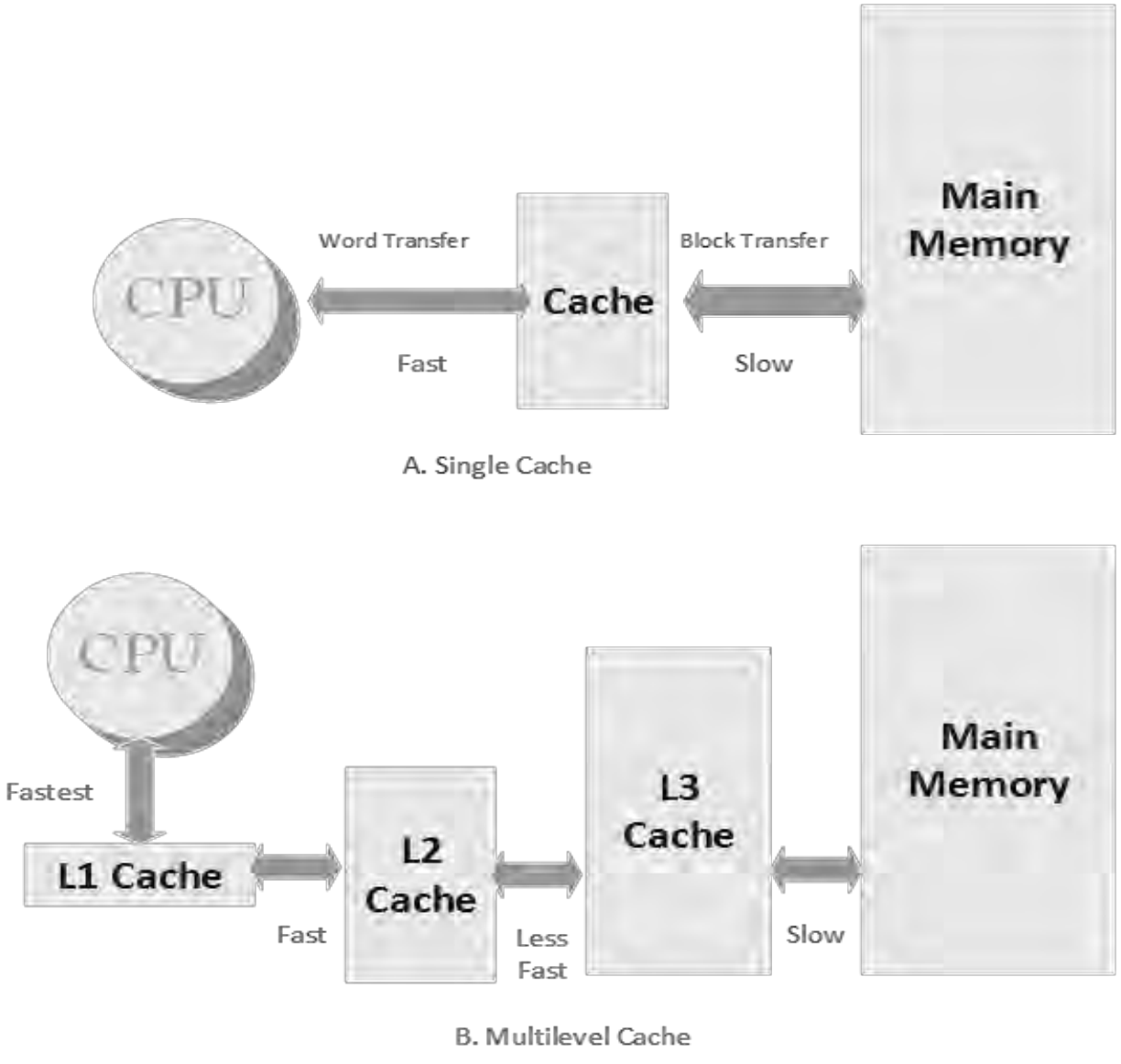

Fig 2. Cache level organization

The L1 caches are typically moved down by a level two (L2) cache. On-chip L2 caches are generally smaller than 512 Kbyte and convey data with a latency of roughly 5 to 10 cycles. If the L2 caches are placed on-chip, an on-chip level three (L3) cache may be added to the hierarchy. On-chip cache sizes differ from 1 Mbyte to 16 Mbyte. They give data with a latency of around 10 to 20 CPU cycles [8] [20].

2.2 LOCALITY OF REFERENCES As a result of restricted size, caches can just hold duplicates of as of recently accessed information or code. Regularly, when new data are stacked into the cache, other data must be replaced. Caches enhance execution and performance just if cache blocks which have already been loaded are reused before being replaced by others.

The reason behind why caches can generously decrease program execution time is the principle of locality of references [7] which expresses that as of late utilized data are prone to be reused sooner rather than future. Locality can be subdivided into spatial locality and temporal locality. An arrangement of references displays temporal locality if recently accessed data are liable to be accessed again soon. An arrangement of references exposes spatial locality if data found near one to another address space in locality have a tendency to be referenced near one another in time [6] [7].

2.3 CACHE MAPPING In this area, we quickly survey the fundamental parts of cache architectures and cache mapping. Data in the cache are stored in cache lines. A cache line holds the information of a contiguous block of primary memory. If the data asked for by the processor are found in a cache line, it is known as a cache hit. Else, a cache miss happens. The elements of the memory block containing the requested word are then fetched from a lower memory layer and replicated into a cache line. For this reason, another data element must normally be replaced. In this manner, keeping in mind the end goal to ensure low access latency, the question into which cache line the data should be loaded and how to retrieve them hence must be taken care of effectively [4] [8]. With respect to hardware complexity, the least expensive way to deal with block placement is direct mapping; the content of a memory block can be set into precisely one cache line. Direct mapped

caches have been among the most mainstream cache architectures in the past are still extremely normal for on-chip caches [8].

However, computer architects have as of recently centered around expanding the set associativity of on-chip caches [4]. An a-way set-associative cache is described by a higher hardware complexity, yet ordinarily implies higher hit rates. The cache lines of a-away set-associative cache are grouped into sets of size a. The elements of any memory block can be set into any cache line of the relating set.

Finally, a cache is called fully associative if the elements of a memory block can be put into any cache line. For the most part, fully associative caches are just implemented as small special purpose caches [4]. Direct mapped and fully associative caches can be seen as special cases of a-way set-associative caches; a direct mapped cache is a 1-way set-associative cache, while a fully associative cache is C-way set-associative, provided that C is the quantity of cache lines.

2.4 PROCESSOR CACHE INFORMATION It is necessary to know the basic details of the processor before actually working on the analysis of cache memory of any architecture. Information such as number of cache levels, cache size of the processor, non-uniform memory access nodes, number of physical processor packages, number of processor cores, number of logical processors etc.

We have calculated all this information using a code snippet [9] which uses the property-1 of C++ and retrieves information about logical processors, related hardware and cache memory information as shown in figure 3. This information is very useful for the processor based analysis of the cache memory at different level L1, L2 and L3.
Property-1: *GetLogicalProcessorInformationEx* [13].

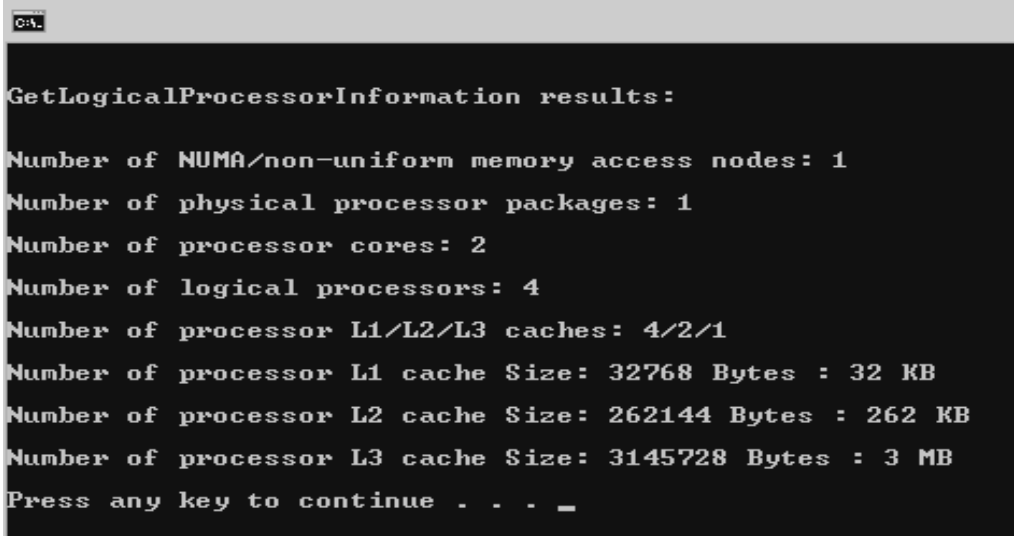

Fig. 3. Processor Cache Information

3. MEASURING AND SIMULATING CACHE BEHAVIOR

In general, examining tools are utilized as a part to figure out whether a code runs productively, to recognize execution and performance issues, and to guide code optimization [10] [11]. With the complexities of digital signal processor applications and the system memory they utilize, it is often very difficult for the developer to understand where and when processor memory accesses are occurring. This is further complicated by the fact that many processors have incorporated cache into the on chip memory. While there are many issues with system memory optimization, the first of those issues needing to be addressed are cache analysis, visualization, and optimization. It is very necessary to analyze the cache using cache tool and by using various analysis to check the system performance [10] [11].

The cache analysis provides developers of any processor system with the benefits of optimization of programs and to improve power consumption efficiency of the entire system.

To demonstrate a cache importance we have implemented simple applications in Asp.net and C#.net which illustrates the cache working and importance of cache.

3.1 SIMULATION CASE - 1 The simulation case-1 differentiates the two systems, Software program using cache memory and without using cache memory. Program-A algorithm shows the code flow for a data access from a lower memory consider access database while program B flow describes the steps for a data accessed from cache named “Sample”. The program A actually retrieves the data from a lower memory with the steps by establishing connection to the lower memory using OLEDB connection driver, requesting lower memory for a required data using a database query, fetching requested

data from lower memory and loading that data on a user page. All this steps actually takes a considerable amount of time. At the same time a memory blocks get allocated for the cache to store this data. In Program A, we have stored this data in a cache named 'Sample' and the same cache and its data we are using in page-two program B.

Program – A - algorithm

- Establishing connection to the database.
- Requesting a database for a required data.
- Fetching required data from the database.
- Retrieving and loading the data to the user on page-one.
- Save the data to the cache named "Sample".

Inversely in program B, we are retrieving same data from the cache memory to load the page-two. The demonstration actually illustrates the time required to execute both the programs and to load both the pages one and two respective to the output of Program - A and Program - B.

Program – B – algorithm

- Requesting a cache "Sample" for a required data.
- Retrieving and loading the data to the user on page-two.

3.2 ANALYSIS OF SIMULATION The simulation illustrates the time required to execute both the programs A and Program B and to load output of both the programs. Program-A output and program-B output shows same data while the time result shows the actual time required to retrieve that data and to output the program. The simulation Figure 4 shows that,

Time taken to load page 1 = Average 6 milliseconds

Time taken to load page 1 = 0 milliseconds (less than milliseconds i.e. in nanoseconds or less)

The graph-1 is plotted on the basis of these results that show how fast machine performance is when it comes to a cache.

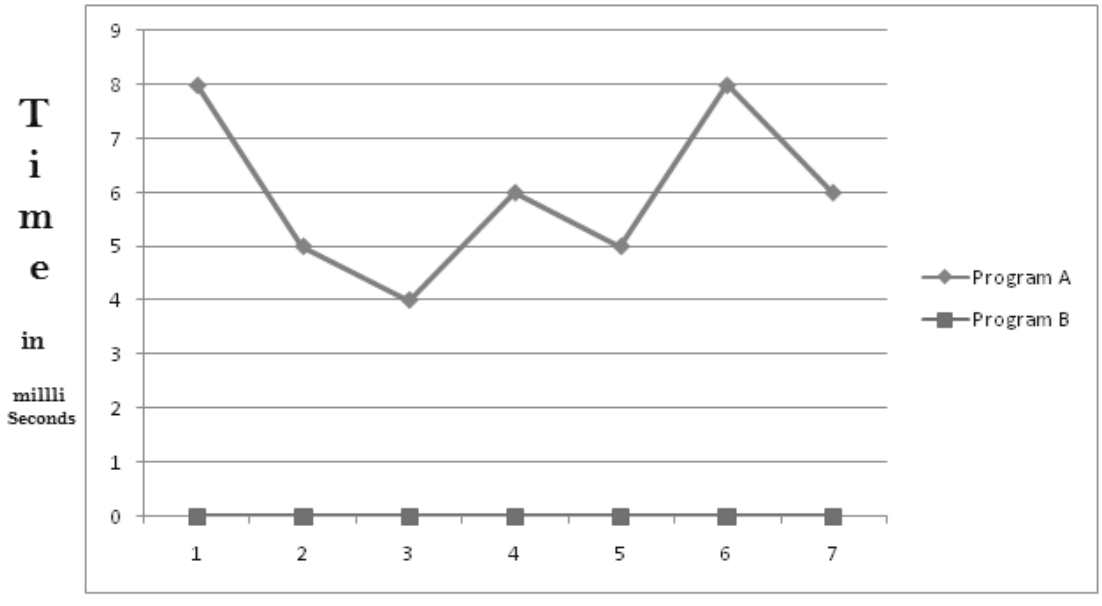

Fig.4.Cache working results for Program A and Program B

4. TECHNIQUES FOR IMPROVING CACHE EFFICIENCY

Before developing any software, programmer should ask below questions about Cache. Does cache matter while developing and using any software? The below work will answer for this questions about cache optimization and coding.

Cache optimizations are required to overcome cache misses and conflict across various mapping policies. It improves the performance of the cache and brings the memory access latencies down which in turn speeds up the memory fetches, minimizes cache misses, miss penalty rate such that the memory system can deliver data near to the CPU clock cycle rate. Operating systems, databases, file systems, even our own software creations all use some sort of cache. Here we have described the cache optimization examples to help define realistic expectations regarding CPU Cache Optimization [4].

4.1 SIMULATION CASE-2 Let's compare two similar C# programs, Program C and Program D. The only difference is the definition of the structures, with Program A having unused members (c and d) as shown below in Program-C and Program-D.

Program - C

```
class Program
{
   struct MyDATA
   {
    public int a;
    public int b;
   }
   static void Main(string[] args)
   {
      MyDATA[] myDt = new MyDATA[10 * 1000 * 1000];
      for (int i = 0; i < myDt.Length; i++)
      {
         myDt[i] = new MyDATA();
         myDt[i].a = myDt[i].b;
      }
   }
 }
```

Program D

```
class Program
{
   struct MyDATA
   {
    public int a;
    public int b;
    public int c;
    public int d;
   }

 static void Main(string[] args)
   {
 MyDATA[] myDt = new MyDATA[10 * 1000 * 1000];
      for (int i = 0; i < myDt.Length; i++)
      {
         myDt[i] = new MyDATA();
         myDt[i].a = myDt[i].b;
      }
   }
}
```

It could be concluded that both programs should run at the same speed as both are doing the same exact processing and there is no obvious reason why a modern compiler would not generate the same binary code for the loop. Running the example on a small PC (a Windows 8.1 machine with a core i3 @ 1.40GHz), with full compiler optimization turned on (in release mode), we get the following results:

1. Program C executed in 139 milliseconds.
2. Program D executed in 197 milliseconds.

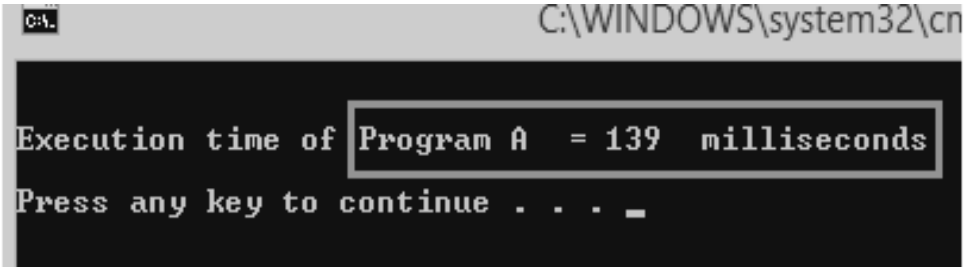

Fig 5. Cache working results for Program C

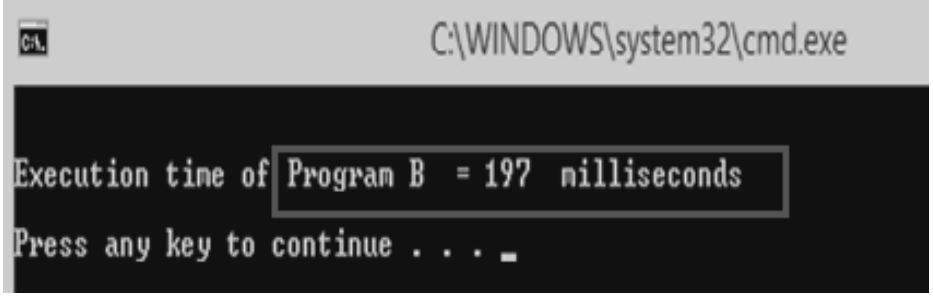

Fig. 6. Cache working results for Program D

Program D allocates twice as much data from memory than Program C, yet it just uses 50% of it (int a, int b). Program execution results confirm the hypothesis theory with a degradation of performance around 30%.

Programmers normally make a supposition; when loading a integer in a cache, it is assumed that 32 bits get copied to CPU's cache memory from memory. But, these CPU caches don't handle exact level of details about memory. Rather, they bring and store memory utilizing altered size pieces. In any case of data-type, bit, integer or long; modern processors load not only an assigned data but also a 64 bytes of data around it. This is called a cache line and a regular cache line is 64 bytes in length [12].

For a Program D, the memory is organized as follows;

a	***b***	***c***	***d***	***A***	***b***	***c***	***d***	***a***	***b***	***C***	***d***	***a***	***b***	***c***	***D***

Fig. 7. A full 64 byte cache line for program D. Every block represents a 32 bit integer.

Each fetch from the memory brings one similar cache line to the CPU Cache. However, Program D only uses the ‘a’s and ‘b’s, so only half of the fetched data is actually used. The amount of data brought into the cache line that is actually used is only 50%. Looking at Program C, the memory is organized as shown in figure 8:

a	***b***	***A***	***b***	***A***	***b***	***a***	***b***	***a***	***b***	***a***	***b***	***a***	***b***	***a***	***B***

Fig. 8. A full 64 byte cache line for program C. Every block represents a 32 bit integer.

Each fetch from the memory brings in only ‘a’s and ‘b’s. Accordingly, the entire fetched data is used. In this case, the fetch utilization is 100%. Program D brings twice as much data from memory than Program C, but it only uses half of it, even if reading the source code let us believe otherwise. Our benchmark run results confirm the theory with a degradation of performance of about 30%. This example highlights a crucial point: a program’s efficiency is defined by how well the developer knows memory access paradigms, such as vector, arrays, lists, etc. But in every case, we assume the cost of accessing data is directly proportional to its size. Unfortunately, considering the cache line unit of higher level memory access for the CPU caches adds an extra level of complexity.

For Simulation Case – 2, we have taken outputs of execution time for a program C and program D about 9 times and plotted it on a graph. The below Fig.9 graph-2 describes the fetch utilization for program C and program D respectively.

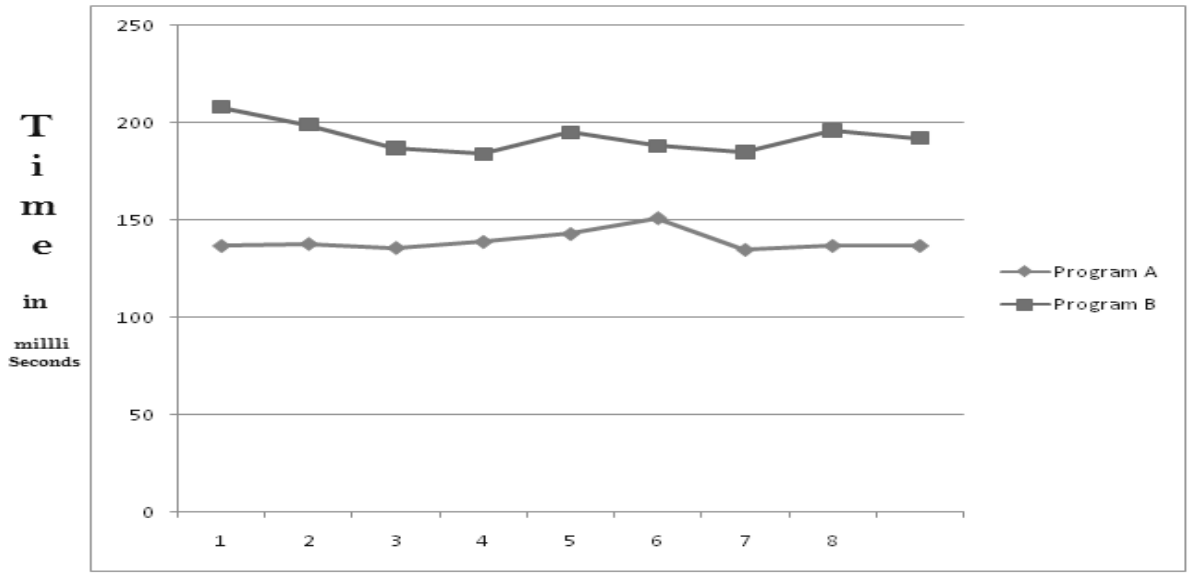

Fig. 9. Graph-2: Result plot for Simulation Case-2

4.2 SIMULATION CASE-3 High data computation serial applications must be explored and investigated for CPU cache issues when the data size is more exceeded the accessible cache size. For multi threaded programs on shared memory frameworks, how the data is moved between caches is frequently a more of an issue than data size.

The Simulation Case-2 illustrates that cache lines can lead performance degradation if the fetched data is not completely used (char c and char d). But, examining the code by only visual scanning for unused variables and data is not generally enough to find such performance degradation. For instance, the simulation case-3 shows Program-E and Program-F both have the same measure of unused information (int b and char c). But if we switch only one line of code (int b and char a) in the declaration of structure, Program F runs more than 50% faster.

Program-E

```
class Program
{
   struct MyDATA
   {
      public char a;
      public int b;
      public char c;
   }

static void Main(string[] args)
   {
      MyDATA[] myDt = new MyDATA[10 * 1000 * 1000];
      for (int i = 0; i < myDt.Length; i++)
      {
         myDt[i] = new MyDATA();
         myDt[i].a++;
      }
      }
   }
```

Program-F

```
class Program
{
   struct MyDATA
   {
            public int b;
            public char a;
      public char c;
   }

static void Main(string[] args)
   {
      MyDATA[] myDt = new MyDATA[10 * 1000 * 1000];
      for (int i = 0; i < myDt.Length; i++)
      {
         myDt[i] = new MyDATA();
         myDt[i].a++;
      }
   }}
```

After execution of Program-E and Program-F we got following results,

1. Program E executed in 171 milliseconds.
2. Program F executed in 117 milliseconds.

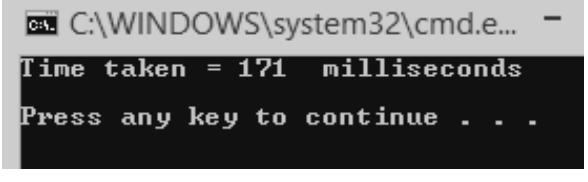

Fig. 10. Cache working results for Program E

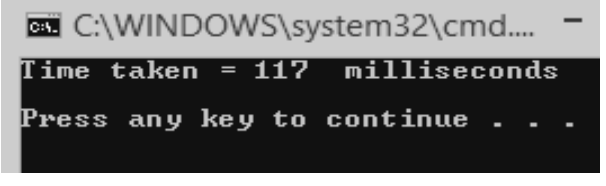

Fig. 11. Cache working results for Program F

In this case-3, compiler allocates data fields in memory based on their sizes and types. A cache line in Program-E resembles the below structure as shown in Fig . Here empty allocations show memory spaces which are wasted because of data arrangement issues.

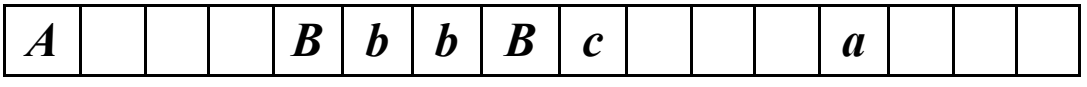

Fig. 12. Cache line due to program-E execution

In Program-F memory is allocated as shown in Fig.

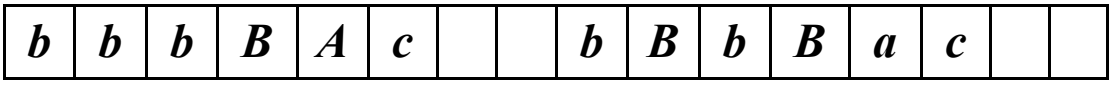

Fig. 13. Cache line due to program-F execution

From this we can see that Program F is clearly using data fetched superior to System E.

In addition, to achieve high levels of cache efficiency, it is necessary to analyze the low level or assembly language code for a given software development. We have calculated hit and miss rate for a sample miniMips assembly code which a developers can use to make the cache analysis.

To know the performance of the code written in low level languages or assembly language, we have referred simulators written in C language [19]. Simulators are of cache architectures and it evaluates performance of a specific code fragment. We have loaded the sample code fragment [19] into the miniMIPs simulator at online simulator [19] assembled it, and executed it. When the breakpoint is reached we have taken the trace of the addressed accessed during execution. This should pop up a dialog with the series of memory addresses accessed by the program. We have copied this address list in a text file trace.txt and used this trace.txt file for further analysis using C-program simulator. We have used the code fragment [19] which simulates a direct-mapped cache with 8 lines of 1 word.

This cache simulator outputs a line for every memory access. When the end of the trace file is reached a summary is printed out.

After compiling and execution the direct-mapped cache simulator given above we output the final number of hits and accesses output by the code. Also, based on the pattern of cache hits, estimated the hit rate of the given miniMIPs code fragment. Similarly we observed the results for a fully-associative cache processor base information.

5. DATA OPTIMIZATION TECHNIQUES

Data access optimizations can be made by utilizing code changes or transformations which change the order in which iteration cycles in a loop nest are executed. The fundamental objective behind these changes or transformation is to enhance temporal locality. The data access optimizations displayed in this segment keep up all data dependency conditions and don't change the after effects of the numerical processing and computation.

Usually, it is hard to choose which combination of changes must be applied with a specific goal to attain to a greatest execution performance. Compilers commonly utilize heuristics to figure out if a change or transformation will be effective or not.

5.1 LOOP INTERCHANGE This transformation turns around the order of two contiguous adjacent loops in a loop nest [10]. As a rule, loop interchange can be applied if the order of the loop execution is not important. Loop interchange can enhance locality by diminishing the stride of an array based processing.

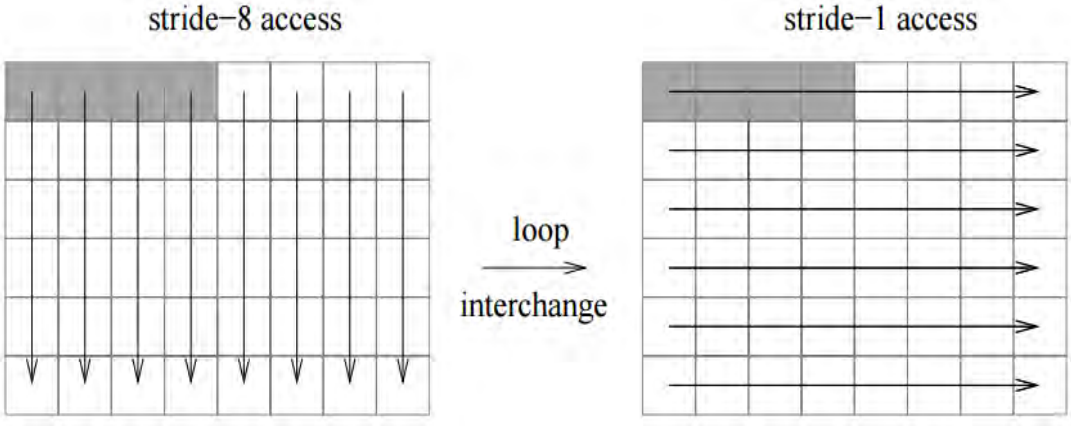

Fig. 14 Access patterns for interchanged loop nests [8].

Original loop nest	Interchanged loop nest
1: double sum;	1: double sum;
2: double a[n; n];	2: double a[n; n];
3: for j = 1 to n do	3: for i = 1 to n do
4: for i = 1 to n do	4: for j = 1 to n do
5: sum+ = a[i; j];	5: sum+ = a[i; j];
6: end for	6: end for
7: end for	7: end for

Algorithm – 1: Loop Interchange [8]

The impact of loop interchange is outlined in Fig. 14. We consider that the array is stored in memory in row order; i.e., two array components are stored nearby in memory if their second indices are successive numbers. The code relating to left part of Fig. 14, on the other hand, accesses the array components in a column wise way.

Hence, the data preloaded in the cache line stamped with grey shading won't be reused if the array is so expansive large, it couldn't be possible fit completely in cache. Nonetheless, after interchanging the loop nest as showed in algorithm-1 [8], the array is no more accessed using stride 8, yet stride 1. Therefore, all words in the cache line are now utilized by progressive loop iterations. This is represented by the right part of Fig. 14.

5.2 LOOP FUSION Loop fusion or combination is a transformation which takes two neighboring loops that have the same iteration traversal and consolidates their bodies into a single loop [12]. Combining two loops brings about a single loop which contains more instructions in its body and consequently offers expanded instruction level parallelism. Besides, one and only loop is executed, in this manner decreasing the total loop overhead by pretty nearly a factor of two.

Original code	After loop fusion
1: for i = 1 to n do 2: b[i] = a[i]+1:0; 3: end for 4: for i = 1 to n do 5: c[i] = b[i] 4:0; 6: end for	1: for i = 1 to n do 2: b[i] = a[i]+1:0; 3: c[i] = b[i] 4:0; 4: end for

Algorithm – 2: Loop fusion [8]

Loop fusion also enhances data locality. Consider that two back to back loops perform global sweeps through an array as in the code demonstrated in algorithm-2 [8], and that the data of the array are so vast it would be impossible fit totally in cache. The data of array b which are stacked into the cache by the first loop won't totally stay in cache, and the second loop will need to reload the same data from main memory. In the event that, if the two loops are joined with loop fusion only one global sweep through the array b will be performed. Therefore, less cache misses will happen.

6. CONCLUSION

Cache analysis gives a mean to visualize the memory and programming execution over time to help the developer to find the area causing cache misses. As a result, cache analysis can be a blue print to applying improvement strategies to enhance cache performance. Code optimization methods and algorithms are approaches to give an efficient cache optimization.

In this paper the techniques and demonstrations given provides the steps important to utilize the cache memory of a given processor. We can see the overall execution performance of a program is enhanced by 30% to 50 % subsequent to use of the optimization algorithms as indicated in the results. The cache analysis addresses the aspects of effective analysis focused at better memory management and helps software developers accomplish efficiency and productivity rapidly, consequently shortening the application development life-cycle and decreasing the time to market for the developer.

FUTURE SCOPE

Performance of software and CPU depends on cache and it increases the speed of memory access by using standard optimization techniques. In future, we will implement most of the cache optimization techniques along with their applications. An optimization technique like loop enrolling overcomes the drawback of the same piece of code being executed multiple times in a loop to decrease the number of loop iterations. Inlining functions can be used to optimize the program by avoiding repetition of function calls. We can write Cache-Friendly Code which has a code design and organization strategy that uses the CPU cache in the most efficient way. In addition, writing Pipeline Friendly Code with optimization leads to better software performance based on the machine's pipeline.

In future, we can have compilers and IDEs that can detect and suggest to the developers a more cache friendly and efficient piece of code instead of their original code.

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COMPARISON BETWEEN SECURITY MAJORS IN VIRTUAL MACHINE AND LINUX CONTAINERS

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ABSTRACT

Virtualization started to gain traction in the domain of information technology in the early 2000's when managing resource distribution was becoming an uphill task for developers. As a result, tools like VMWare, Hyper-V (hypervisor) started making inroads into the software repository on different operating systems. VMWare and Hyper-V could support multiple virtual machines running on them with each having their own isolated environment. Due to this isolation, the security aspects of virtual machines (VMs) did not differ much from that of physical machines (having a dedicated operating system on hardware). The advancement made in the domain of linux containers (LXC) has taken virtualization to an altogether different level where resource utilization by various applications has been further optimized. But the container security has assumed primary importance amongst the researchers today and this paper is inclined towards providing a brief overview about comparisons between security of container and VMs.

Keywords *- docker, hyper-V, linux container, openVZ, sandboxing, virtualization, vmware*

1. INTRODUCTION

The concept of virtualization [1 and 2] was created with the sole intent of managing resource distribution efficiently and hence system resources started getting divided logically instead of physical division. Ever since the introduction of mainframe computers in 1960s by IBM, this technique of logical division has been of great utility. Apart from efficient resource distribution, virtualization has another advantage: it is easier to deal with systems at software level than working on hardware. Hardware virtualization has enabled users to deal with hardware more efficiently via logical connections where a hypervisor emulates a piece of computer hardware.

With the advent of cloud computing [3 and 4], virtualization has assumed primary importance for enterprises as well. It becomes easier to manage data centers across the world and thus it helps in working remotely. As functionality tends to increase for enterprise applications, there has been a disproportionate rise in the number of virtual machines (VMs) on each data center. Each hypervisor had an upper limit on the number of VMs that can run on it. Moreover, most of these applications did not require even half the resources allocated to VM by CPU. Thus, it was mandated with growing number of applications to run two to three times more server instances on a given server as compared to VMs. This lead to the development of linux containers (LXCs) [15 and 16] wherein only those resources will be used which are required by applications.

Although LXCs has been used efficiently in successfully executing various enterprise level applications, the security features of LXCs are yet to evolve when compared with VMs. Due to the isolation provided in VMs the threat of intrusions has been neutralized to a great extent via intrusion detection algorithms [5, 6, 7 and 8]. Furthermore, all the security aspects pertaining to detection of spam [9] and malware [10 and 11] which have been addressed in VMs are yet to remain addressed in containers. Although each LXC receives its own network stack and process space as well as its instance of file system, it doesn't have its own user namespace. As we proceed further we'll look at various container based technologies how security features varies across LXCs and VMs.

2. CONTAINER BASED TECHNOLOGY

Linux containers (LXCs) provide operating system-level virtualization and they have their own process and network space. Although work is still going on in creating a separate user namespace, the isolation provided in other aspects has been at par with virtual machines. Keeping in view the demand of growing number of instances required along with sandboxing, various container based technologies were designed to address this feature. The two primary container based technologies which we'll look at: docker and openVZ.

OpenVZ: OpenVZ [17 and 18] is a container based technology which allows a physical server to run multiple instances of an operating system called containers or virtual private servers (VPS). Each container has its own network stack, serial ports, process tree and file system. In later versions of openVZ, work is being done to create container's own user space. It uses single patched linux kernel and can run only linux. It might be disadvantageous to use openVZ in case containers need different kernel version since all openVZ containers share the same architecture and kernel version. Also since it doesn't carry the overhead associated with operating system, it is much more efficient, scalable. Furthermore, there is dynamic memory allocation i.e. the memory allocated to 1 linux container can be used for other container as well without the requirement of rebooting the entire system.

Docker: Docker [14] is different from openVZ in the sense that former sees a container as an application/service while latter sees container as a VPS. Since container is a single application in docker's terminology, it is important that interface between various containers needs to be robust since multiple containers might be required to run an application. For instance, in order to run a particular application, we might need configuration files from 1 container and database from another container. Thus, it is important to have secure and robust communication between two containers. Since each container has its own network stack, the secure communication between 2 containers can be achieved via any of the following protocols: SFTP [19], SSH [20], FTPS [21 and 22] and SCP.

Docker also has the capability of importing/exporting containers via access to the public registry. Moreover, docker defines an API for automating and customizing the creation and deployment of containers. It also has the capability of tracking and managing successive versions of a container, inspecting diff between versions, committing new versions, etc. Apart from this it has similar features compared to openVZ where it provides namespace, file system, network, resource isolation. Furthermore, docker also provides logging feature where the standard streams of each process container is collected and logged for real-time or batch retrieval. Lastly, docker provides an abstraction layer for containers so that they can run on different operating systems without any compatibility issues.

3. COMPARISON BETWEEN CONTAINERS BASED TECHNOLOGY AND VIRTUAL MACHINES

Linux containers were designed with a single view of managing CPU resources distribution more efficiently. On any instance of VMWare [12] or Hyper-V, it is difficult to run more than 10 VMs due to the overhead incurred. Containers have resolved this problem to a great extent where they only make use of resources which are required by the application or service. Thus, more than 50 instances of container can run on single quad-core machine. Let's consider the example of any enterprise email security product: its main functionality would be to scan emails for spam/virus/malware, manage logs [13], manage message transfer agent (MTA) and report any datacenter outage in case the product is deployed on cloud network. In most cases, these functionalities described will not make any use of kernel data structures or operating system libraries or any related dependencies. Thus, rather than having VMs for each aspect of the product, it's better to containerize each feature by sandboxing them using docker/openVZ. In many of the organizations, VMs are emulated so as to perform feature testing which consumes hordes of memory space and CPU utilization. Having containers would ensure that redundancy would not have much impact on the resource consumption. Scalability would be easier since the time required for container installation is much less as compared to VMs.

On the other hand security aspect of docker/openVZ has been of concern lately. As isolation reduces, security is bound to decrease exponentially. Since containers share the same operating system and kernel, it is easier to gain access to containers especially as root user on linux. Although docker isolates many aspects of the underlying host from an application running in a container from an underlying host, the separation is not as strong as that of VM. Moreover, some applications might need to run on different operating system which is not possible in containerized technology.

Keeping in view the advantages and disadvantages of LXCs/docker, we need to arrive at some kind of trade off. The ideal situation would be to have few VMs installed on physical machine and then have many instances of container running on VM. This would ensure that security features of VM along with optimized features of LXCs would give maximum performance for a system. In case of cloud networks having data centers around the world, few VMs can be installed on a base machine on every datacenter followed by running multiple instances of LXCs on those VMs. Since resource consumption would reduce drastically, this solution would be cost effective for many organizations.

4. CONCLUSION

The manner in which virtualization has dominated over the past decade goes on to show how important the role of linux based containers will be in future. This is evident from the fact that many organizations like Amazon, Microsoft have already adopted this technology in their cloud based products. Furthermore, the scalability which is being offered by the container technologies would ensure that cost savings would grow manifold in the near future. In this paper, a brief overview was provided about docker, openVZ: two container based technologies which are often seen as potential replacement for VM. In addition, a comparison was provided between LXCs and VMs from general as well security point of view.

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DESIGN AND SIMULATION OF STRIPLINE-SLOTLINE TRANSITION FOR ULTRA WIDEBAND APPLICATIONS

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ABSTRACT

An ultra wideband stripline-slotline transition has been designed and simulated in this paper. The achieved bandwidth is 9:1 with reflection coefficient better than -15 dB over the entire range. This transition is extremely useful in the antenna feed networks and miniaturized microwave circuits where efficient transition is required from stripline to slotline. The transition is achieved by stub-cavity matching which also acts as a balun and can operate over wide multi octave bandwidths.

Keywords- *Stripline-Slotline transition, stub, cavity and balun.*

1. INTRODUCTION

The transition between microwave transmission lines is a subject of great interest among researchers. Many researchers have reported and provided mathematical analysis of broadband microstrip-slotline transition using stub-cavity matching [1]. An analysis and design of ultra wideband stripline-slotline matching has been provided in this paper.

For any broadband microwave system operating from f_1 GHz to f_2 GHz, the centre frequency (f_c) can be defined as:

$$f_c \frac{f_1 + f_2}{2} = \text{GHz} \quad (1)$$

All the design parameters for a broadband microwave system are generally calculated at the centre frequency so that the performance doesn't vary beyond the permissible limit.

To match the input impedance of a transmission line to the load impedance, the most widely used technique is quarter wave transformer. The quarter wave transformer is easy to design but can't be used for broadband applications as the size of quarter wave transformer is frequency dependent. A general broadband quarter wave transformer for stripline-slotline transition can be designed using stub-cavity matching. In stub-cavity matching, the orthogonal crossover of stripline and slotline is employed where radial stub is provided at the end of the stripline while cavity is provided at the end of the slotline [2]. A typical geometry of such transition is shown in Fig. 1.

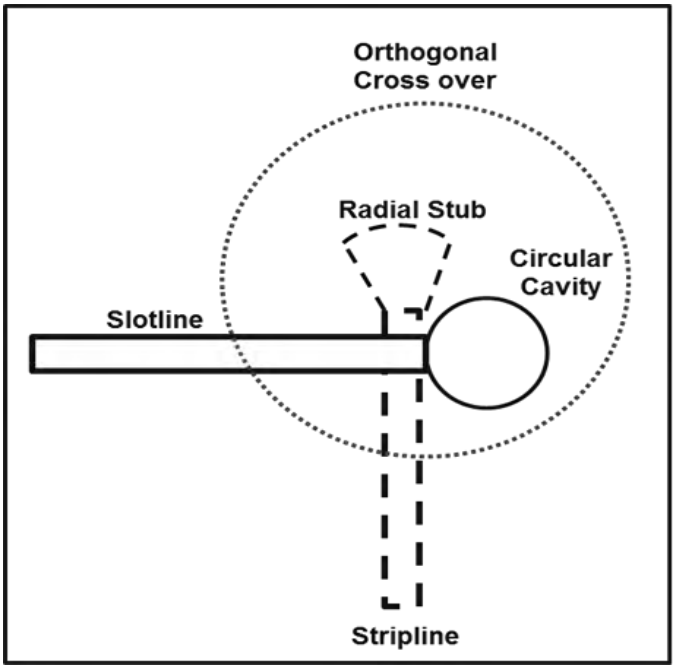

Fig. 1 Stripline-Slotline Transition

2. DETAILS OF PAPER

From the transmission line theory [3], the input impedance of a lossless transmission line in open and short condition can be defined as:

$$Z_{in\ open} = -j\ Z_0 \cot \beta l \quad (2)$$

$$Z_{in\ short} = j\ Z_0 \tan \beta l \quad (3)$$

Where,
β = propagation constant = $\frac{2\pi}{\lambda}$

l = length of the transmission line

Z_0 = characteristic impedance of the transmission line

The variation in the input impedance of a transmission line under short and open condition is depicted in Fig. 2. Here the term βl defines the electrical length of the transmission line and concludes that for shorted transmission line the input impedance is inductive and it appears open for the electrical length of $\frac{\pi}{2}$ or physical length of quarter wavelength. In the same manner, the input impedance of open transmission line is capacitive in nature and it appears short at the electrical length of $\frac{\pi}{2}$ or physical length of quarter wavelength. If the electrical length of the transmission line exceeds $\frac{\pi}{2}$ (or physical length exceeds quarter wavelength), the input impedance of the transmission line in shorted condition becomes capacitive while in open condition it becomes inductive.

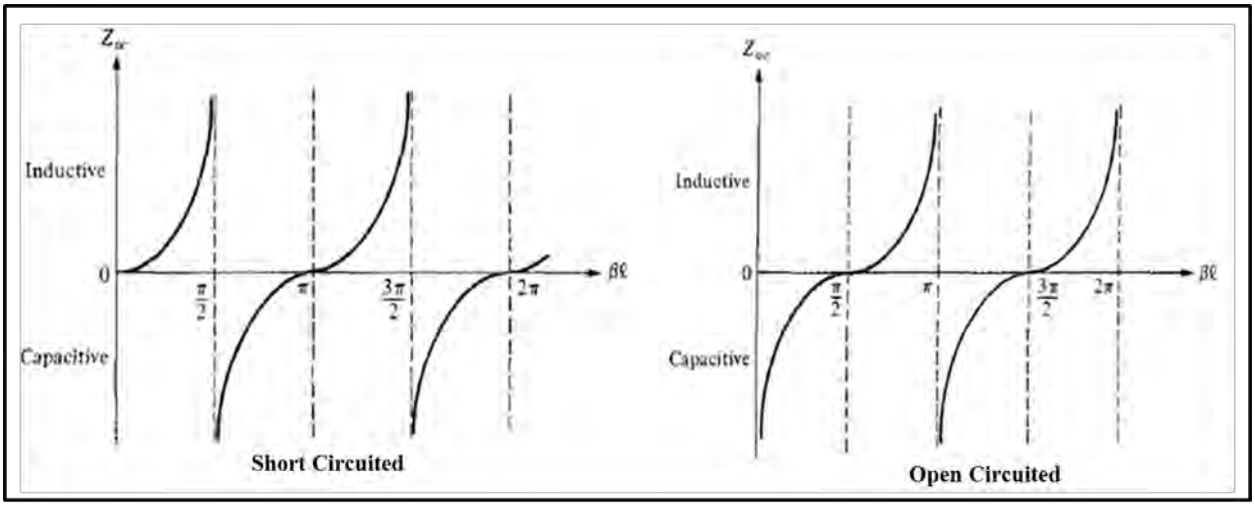

Fig. 2 Input impedance of lossless transmission line

The radial stub and circular cavity at the represents open and short circuit respectively but when the impedance is seen from the distance of quarter wavelength, the open stub at stripline end acts as virtual short while the circular cavity at slotline acts as virtual open. The range of frequencies for which the length of the radial stub and circular cavity is less than quarter wavelength, the stub represents capacitive reactance and the circular cavity represents inductive reactance. If the length of the radial stub and circular cavity is greater than quarter wavelength, the stub represents inductive reactance and the circular cavity represents capacitive reactance. Therefore, the impedance matching is achieved by series-shunt stub over a wide range of frequencies. Equivalent circuit for stub-cavity matching is shown in Fig. 3.

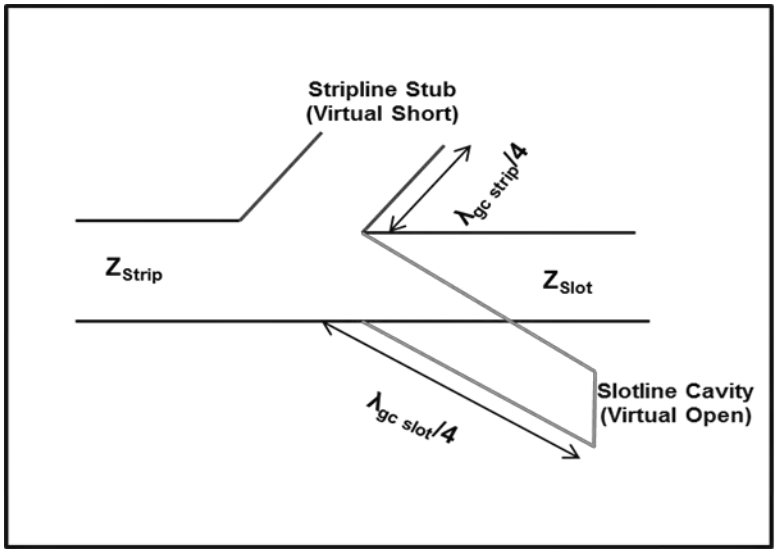

Fig. 3 Equivalent Circuit for Stripline-Slotline Transition

3. DESIGN PARAMETERS

At centre frequency i.e. 10 GHz for 2-18 GHz band, the free space wavelength can be calculated as:

$$\lambda_{0c} = \frac{300}{\text{f (GHz)}} = \frac{300}{10} = 30 \text{ mm} \tag{4}$$

The guide wavelength in stripline and slotline for 10 GHz in RT Duroid 5870 substrate is:

$$\lambda_{\text{gc strip}} = \frac{30}{\sqrt{\varepsilon_{\text{eff strip}}}} = \frac{30}{\sqrt{2.33}} = 19.65 \text{ mm} \tag{5}$$

$$\lambda_{\text{gc slot}} = \frac{30}{\sqrt{\varepsilon_{\text{eff slot}}}} = \frac{30}{\sqrt{1.665}} = 23.25 \text{ mm} \tag{6}$$

The quarter wavelengths for free space, stripline and slotline at 10 GHz comes out as 7.5 mm, 4.91 mm and 5.81 mm respectively. Therefore, the radius of radial stub is taken as 4.9 mm and the diameter of circular cavity is taken as 5.8 mm. Another important parameter is stub angle because it affects the ripple in the pass band. The stub has been flared in both the directions with different angles to reduce the mid band ripples. It is also found that the transition givers better performance when elliptical cavity is used instead of circular cavity at the end of the slotline [4]. Based on the calculated values, a CAD model of stripline-slotline transition has been developed and simulated (as shown in Fig. 4) using CST Microwave Studio 2011.

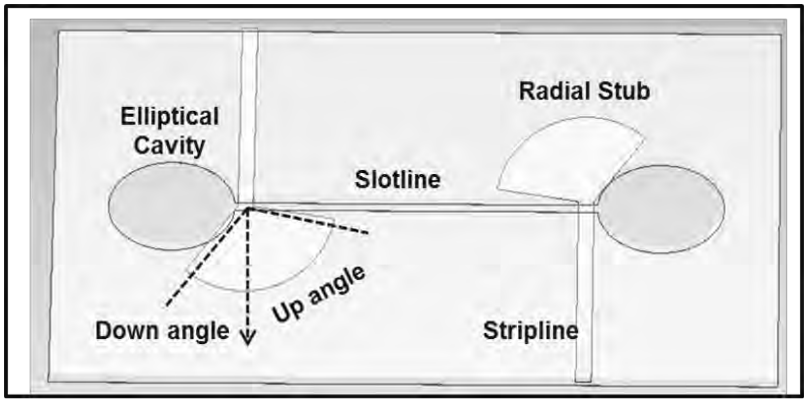

Fig. 4 Simulated model of Stripline-Slotline Transition

The optimized values of design parameters have been presented in Table 1.

Table 1: Design Parameters		
S. No.	**Parameter Name**	**Parameter Value**
1	Stub Radius	5.1 mm
2	Cavity Major Radius	3.6 mm
3	Cavity Minor Radius	2.2 mm
4	Stub Up Angle	80^0
5	Stub Down Angle	35^0
6	Length of Transmission Line	21 mm

4. CONCLUSION

A broadband stripline-slotline transition has been presented in this paper with appropriate design equations and design parameters. The simulated result shown in Fig. 5 validates the theoretical model of the design and shows that the transition works well for 9:1 bandwidth. The reflection coefficient is better than -15 dB for the entire range with insertion loss lesser than 1 dB for one wavelength long transmission line.

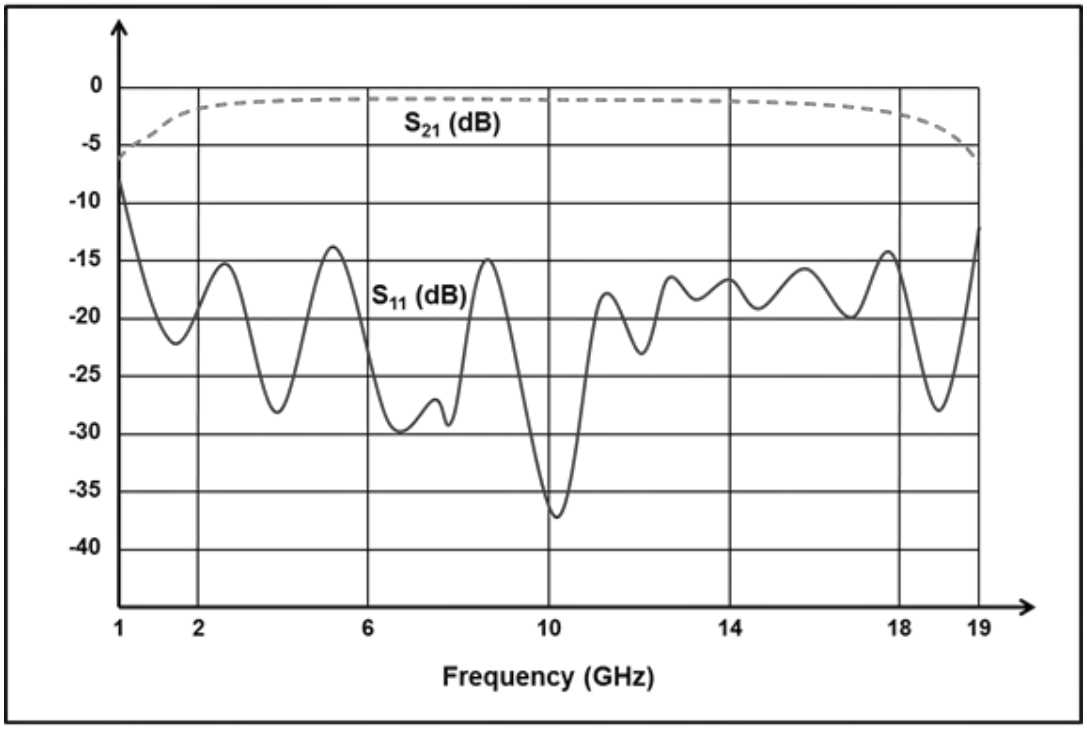

Fig. 5 Simulated Reflection Coefficient & Insertion Loss

The major advantages of this transition are:

- Planar transition from stripline to slotline.
- Low insertion loss.
- Better matching with low reflectivity.
- Easy to incorporate in microwave integrated circuits and antennas.
- Better control over pass band ripples.

5. ACKNOWLEDGEMENTS

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ECONOMIC ACTIVITIES ASSOCIATED WITH EXTRACTION OF RIVERBED MATERIALS IN THE TINAU RIVER, NEPAL

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ABSTRACT

A study was conducted during 2012 to 2013 in the selected reach of Tinau River, Nepal. The main objective of the study was to quantify employment and income generation from extraction of construction materials from the river. A 10 km stretch of the river was selected for the study. Sample survey with semi-structured questionnaire and field observation were the main tools used during field investigation. Extraction of riverbed materials from the banks, beds and floodplain areas of the river has provided many kinds of job opportunities for the people living in the vicinity of the river. It has also generated adequate amount of revenues. The collected revenue has been invested for many kinds of social and infrastructures development for years. Though extraction of riverbed materials is beneficial for income and employment generation, it also has negative environmental impacts in and around the river. Furthermore, the study concluded that riverbed extraction should be continued with special monitoring and evaluation in the areas where there is still room for extraction.

Key words: *Extraction, Crusher plants, Economic activities, Tinau River*

1. INTRODUCTION

Rivers have been used for various purposes since past decades. Rivers and river banks reflect the cultural heritage and economic prosperity of the people living there. Rivers are also the symbol of gods and goddesses especially for Hindus and Buddhists in Nepal. Rivers reflect peoples' respect for nature, environment and their understanding of the ecological processes [1]. There are many large rivers throughout the world such as the Sepik, the Mississippi, the Volga, the Zambezi, the Mekong, the Ganges, the Danube, the Yangtze, the Nile and the Amazon [2]. These rivers are not only the genesis of human civilizations but also the means of transportation, resource generation and promotion of tourism development [3, 4]. Due to various natural and anthropogenic causes, such rivers are being disturbed by several factors. Urbanization, along with industralization have been degrading the ecology of many rivers [5, 6]. This type of disturbance affects the river continuum process too [7, 8].

There are over 6000 river and rivulets in Nepal. Tinau River is one of them. Tinau River carries lots of sand and gravels. As the river enters into the Terai Region of Nepal from the hills, it deposits the material. These materials are being used by the local administrative bodies such as Village Development Committee (VDC), municipality and District Development Committee (DDC). These local administrative bodies are generating millions of Nepalese Currency for years [9]. However, the extraction of riverbed materials is not going on in a scientific way [9].Thus, the ecology of the river is degrading.

Aquatic ecology of Tinau River has been altered due to human activities such as excavation and extraction of construction materials for the last decade. Tinau River has been facing both external and internal degradation for years. External degradation is increasing with the pace of increasing population of this region, whereas the internal devastation is caused by geo-environmental degradation of Tinau River basin [10]. The external degradation includes impacts on water quality, non-treated and non-regulated foul water discharge into the river, dumping of garbage in the river floodplain areas, encroachment of floodplain areas as well as uncontrolled extraction of riverbed materials [11,12].

In Nepal, local self governance act and local self governance regulations provided the right to extract the natural resources for the income generation within their political boundaries [13, 14]. Since then, massive extraction of construction materials started without considering adverse environmental consequences. The extraction of construction materials from the beds, banks and floodplain areas of the Tinau River has disturbed its ecology. However, it has generated a lot of employmant opportunities for the people living in this locality.

2. MATERIALS AND METHODS

The study was conducted during the period of 2012-2013 in the Tinau River from Paschim Amawa VDC to Bethari (Gonaha VDC). Around 10 km stretch of Tinau River was selected for this study (Fig. 1). The study was based on field survey. Semi-structured questionnaire was prepared for field investigation. Labors in the extraction activities, industrialists and the businessmen of the study area were taken for sample survey. In every port of entries (Naka) of the extraction zone 48 labors were selected randomly for interview. Similarly, businessmen and industrialists were also selected for the interview. Besides, some old-aged persons from the study area were questioned. Total of 90 persons were selected for interview. Out of 90, 48 were labors, 10 were businessmen, 17 were industrialists and 15 were age old inhabitants. The focused group discussion (FGD), seminar and interaction were held for appropriate data collection for this study. By the end of sampling, it was cross checked for the validation of collected data. The data was processed using software Excel. Pie chart, Bar Chart and Tables were used for presenting primary and secondary data.

The length of Tinau River is 95 km, and total catchment area is 1081 km2 [9]. There are many tributaries of Tinau River but the major are: Jhumsa Khola, Sisne Khola, Bhaiskatta Khola and Dobhan Khola [3, 15]. However, the study was conducted only in a small stretch (10 km.) of the river. The river originates from the Palpa district (Mountainous region) and flows through the plain area (Terai) of Rupandehi district. The study covers only some parts of the Terai region of Rupandehi district (where there is sufficient riverbed materials deposited).

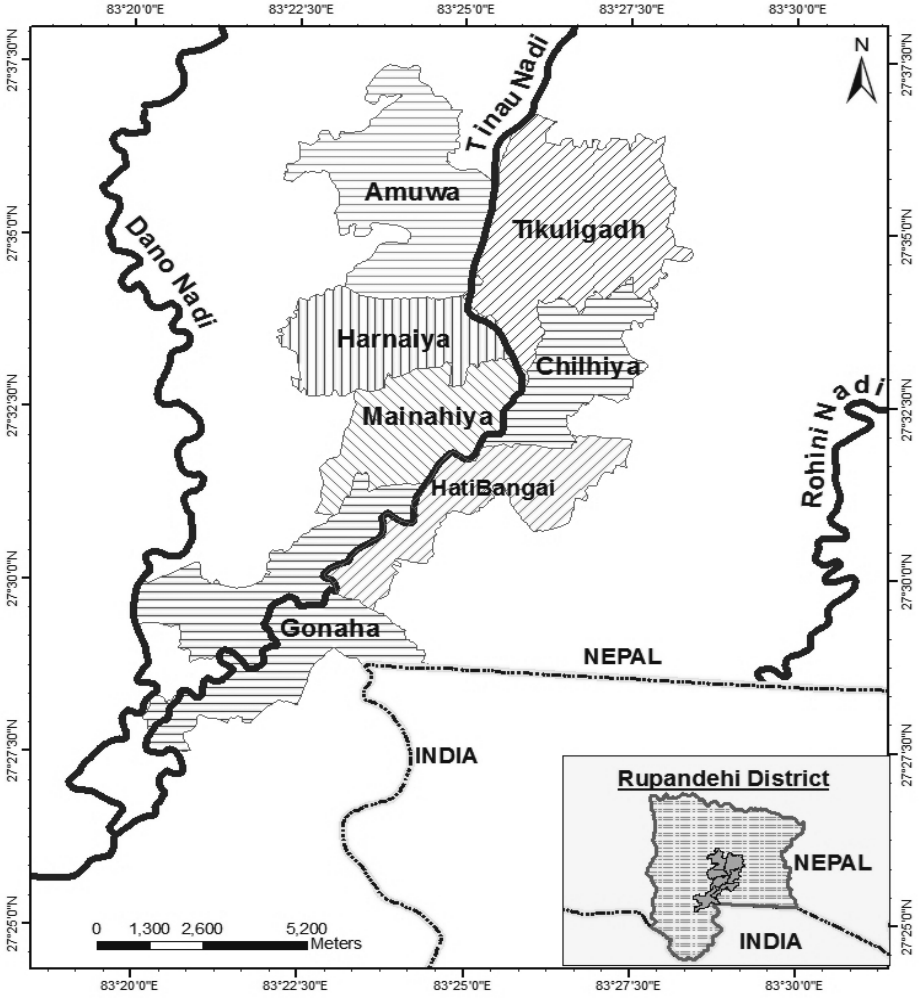

Fig.1: Map showing study area **[16]**

3. RESULTS AND DISCUSSION

3.1 RESULTS There are 17 ports of entries (NAKAs) along the bank of Tinau River. But there were only 10 NAKAs running during the period of 2012. The main existing NAKAs and their status are presented in table (Table 1). These NAKAs are open for extraction of riverbed materials as the environmental impact assessment (EIA) report of DDC.

Table 1: Details of NAKAs

Name of Rivers	Name of VDCs	Open Ports (Naka)	Total Extracted Quantity, cft.
Tinau	Tikuligadha	Baghdhuranaka	755400.00
		Jeetpurnaka	736400.00
	Chilhiya	Kawanaka	0.00
		Sonaret	0.00
	Hati Bangai	Mahuwari	564400.00
		Bairihawa	569700.00
	Mainahiya	Kutta	171000.00
		Bargadawa	58600.00
	Harnaiya	Bhaisakhadar	433500.00
	Pa. Amuwa	Kanari	685255.00
Grand Total, Cubic Feet			**3,974,255.00**

The extraction of riverbed materials has generated self employment. There are some new businesses such as hotels and groceries emerged due to riverbed extraction along the bank of Tinau River. These businesses have provided employments for adequate number of people. The details of employment generated from the hotels and groceries (Kirana Pasal) are presented in table 2.

Table 2: Employment generated from the hotels and groceries (KiranaPasal)

S.N	Name of "NAKA "	Type of Business		Establishment.	Business pattern Sea-sonal/ Yearly	No. of human resources engaged	Investment (NRs.)
		Hotel (H)	Groceries (G)				
1	PashimAmuwa, Bar-dahawa	H	-	2008	Seasonal	2	23000.00
2	PashimAmuwa, Kanari-Chowk	-	G	2012	Yearly	5	40000.00
3	PashimAmuwa, Kanari	H	-	2009	Seasonal	3	30000.00
4	Shankarnagar, Dingernagar	-	G	2010	Seasonal	2	15000.00
5	Shankarnagar, Yogikuti	H	-	2011	Seasonal	4	50000.00
6	Aanandavan, Pauni	H	-	2005	Seasonal	3	12000.00
7	Aanandavan, Gorkatta	H	-	2008	Yearly	4	40000.00
8	Motipur, Sauraha	-	G	2010	Seasonal	2	12000.00
9	Bhaisakhadar, Harnaiya	-	G	2007	Seasonal	4	22000.00
10	Kutta, Mainahiya	H	-	2003	Seasonal	2	12000.00

The deficit of construction materials has directly created a negative impact on new emerged businesses along the bank of Tinau River. During survey, five hotels and three groceries were found to be in danger. These businesses were in loss and about to be closed. However, one hotel and one grocery have only minor effect and could run in extreme conditions too. The investment pattern of business along the selected stretch on the bank of the river is presented in Fig. 2.

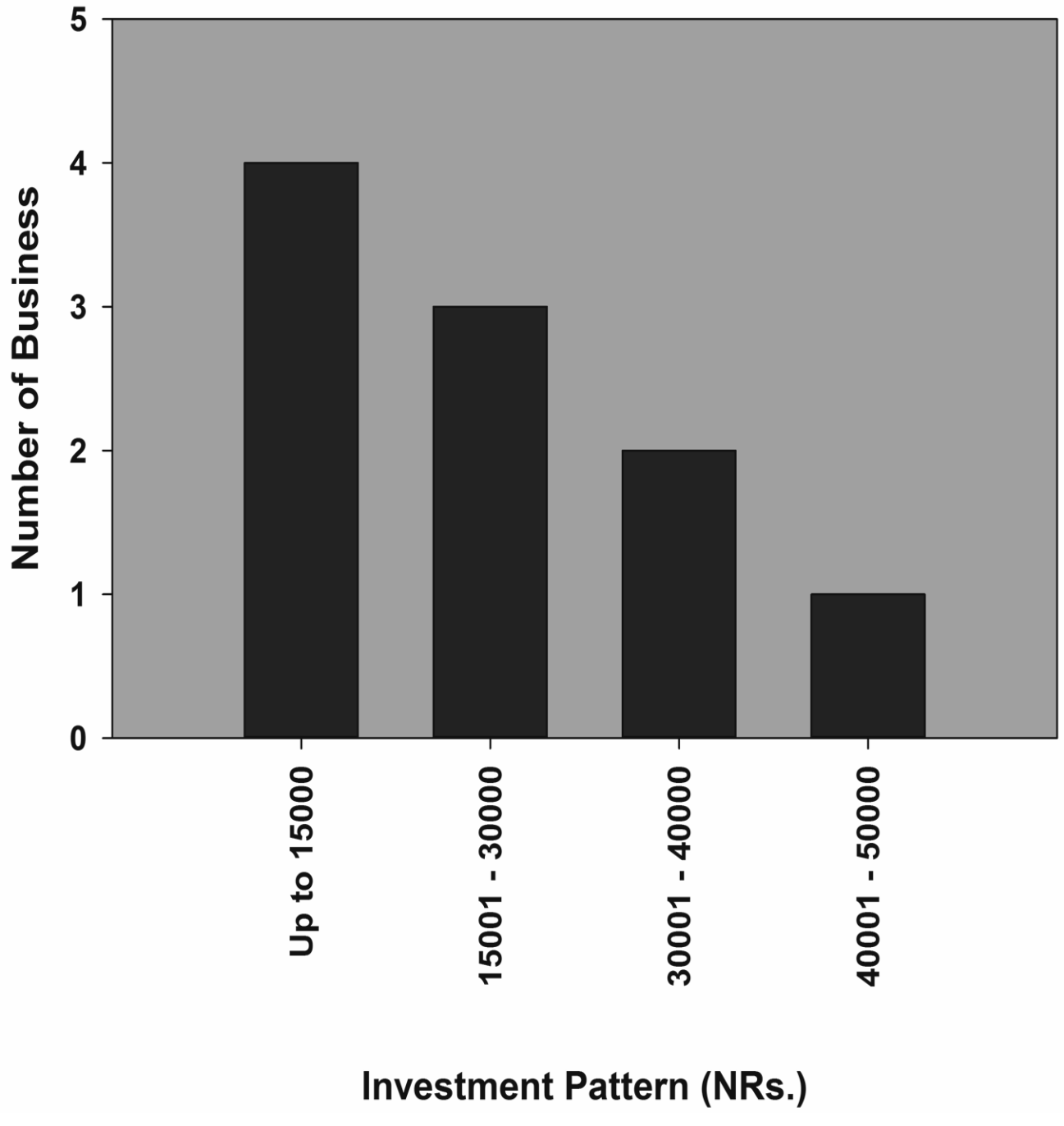

Fig.2: Investment pattern of business in the bank of Tinau River

There are altogether 17 crusher plants along the banks of Tinau River. But all plants are not in good economic condition. During survey the owners of the crusher plants reported that they had major effects on income generation due to shortage of construction materials and ban on the extraction activities from the Tinau River basin. As a result, some plants run seasonally and only a few run all weather. The details of crusher plants are presented in table 3.

The crusher plants have earned millions of Nepali Currency from the finished and unfinished materials. These industries have not only earned huge amount of money but also provided the job opportunities for hundreds of people (Table 3). Similarly, industries have stopped people from going to the foreign countries such as Malaysia, Qatar, Dubai, South Korea, etc. for job opportunities to some extent. Thus, these industries would be much more beneficial for us if we let them run under controlled mechanism sustainably.

Table 3: Income/loss, investment and employment generation from crusher plants

S.N	Name of Industries	Type of Business (Seasonal/Yearly)	Employment generation	Yearly Income/Loss (NRs.) '000	
				Income	Loss
1	Irbin Crusher Udhyog	Seasonal	22		500
2	Super concrete Udhyog	Yearly	24	3000	-
3	Pathak RodaDhungaUdhyog	Seasonal	12	1500	-
4	KalikaRodaUdhyog	Seasonal	10		400
5	Tinau RodaDhungaPrasodhan	Seasonal	50	1000	-
6	ShristhiRodaUdhyog	Seasonal	10	500	-
7	Muktinath Concrete Udhyog	Seasonal	35	4000	-
8	KasyamNamunaRodaUdhyog	Seasonal	30	2500	-
9	SiddheshworikamanarodaUdhyog	Seasonal	50	2000	-
10	Tilottama Concrete Udhyog	Seasonal	25	500	-
11	Pasupati Stone Crusher	Seasonal	15	-	400
12	ChamundaRodaDhunga Industries	Seasonal	18	-	300
13	Shrestha RodaUdhyog	Seasonal	20	600	-
14	New ShristhiNamunaRodaUdhyog	Seasonal	17	700	-
15	Kamana Stone	Seasonal	19	-	700
16	Juntara Concrete Udhyog	Seasonal	10	1500	-
17	Buddha Concrete Udhyog	Seasonal	14	-	500

Although some opportunities had been generated by the Tinau River, the rate of employment generation was decreasing day by day due to shortage of construction materials in the river.

After the ban on extraction of construction materials, some industrialists reported that they were in loss from the industry. The effects of shortage of materials could directly be seen on the employment and income generation. There were large number of labors engaged in the extraction activities. However, their jobs were not secured. The engaged labors were of two types; married and unmarried. During survey it was found that the majority of labors were married (83%) and minority (17%) were unmarried.The income generation by labors from the involvement in the extraction of construction materials is presented in table 4. During survey, age old people of that locality were questioned whether the extraction activities were good. The people answered differently. Eighty percent(80%) of the respondents (age-old people) reported that it was beneficial. Twenty percent (20%) of the respondents reported that the extraction activities should be banned as it degraded the river valley environment. However, hundreds of labors were engaged in the extraction activities. The details of labors, their daily income and working hoursare presented in table 4.

Table 4: Engaged labor and their details of works

S.N.	Age	Daily Income (NRs.)	Working Hours (Per Day)	Working Month (Per Year)
1	28	700	6	6
2	28	500	6	5
3	30	1000	8	5
4	22	600	6	5
5	22	600	6	5
6	21	600	6	6
7	22	600	6	6
8	28	600	6	8
9	45	500	6	8
10	34	500	4	6
11	27	500	4	8
12	18	500	4	8
13	19	500	4	8
14	36	500	4	8
15	19	500	4	8
16	25	500	4	8
17	18	600	4	8
18	18	600	4	8
19	16	600	4	6
20	38	600	4	8
21	17	600	4	8
22	27	600	4	6
23	32	600	4	8
24	30	500	4	8
25	25	700	6	8
26	36	500	6	8
27	39	500	8	8
28	32	600	8	7
29	34	700	8	6
30	41	700	8	8
31	17	500	8	8
32	35	600	8	6
33	40	800	8	7
34	55	500	8	8
35	52	400	8	6
36	40	300	8	5
37	40	350	6	5
38	25	500	8	5
39	15	300	6	8
40	52	600	6	6
41	40	500	8	6
42	41	500	6	7
43	44	250	6	7
44	55	350	5	7
45	56	400	8	8
46	27	700	5	7
47	19	700	8	8
48	16	600	8	7

3.2 DISCUSSION The natural resources like sand, gravel and boulders are good sources of income and revenue generation. Many districts of the Terai (15 districts) and some of mid-hills like Makawanpur, Kavre, Udayapur, Bhaktapur, Kathmandu, Dhading, Kaski and Nuwakot are also the potential districts for riverbed materials [17].

Tinau River is also one of the most important rivers in the western development region. There are altogether 17 ports of entries but eight ports of entries have already been stopped due to lack of raw materials in the river. Though the riverbed materials are more profitable raw materials for crusher industries, the extracted volume was more than the deposited volume [9]. Thus, there is deficit of raw materials.

Sand, gravel, stones (SG&S), and other mined natural resources are the foundations of both the ancient and the modern world. Great structures and wonders of the world would not have been possible without these resources. However, the reckless use of these resources has also led to serious human and property consequences in many countries. Nepal, a mountainous country, has an abundance of SG&S resources which, if utilized judiciously, could help to shape Nepal's development and affluence. However, a balanced outlook on Nepal's SG&S sub-sector seems to be lacking. There are two extreme outlooks – one that tries to accumulate wealth at the cost of the environment, and the other which opts to keep the resources intact and untouched. In this situation, it is imperative for the country to seek a prudent outlook on the sub-sector so that the undesirable extremes of "quick-and-dirty extraction" and "non-extraction" are substituted by "environmentally regulated extraction," for which to become feasible, the sub-sector must be observed and studied thoroughly. This realization has led to the production of this report. Crusher plants are the backbone of income generation of these districts. On average 137 million Nepalese Rupees (NRs.) is generating by DDC from crusher plants [9]. This amount is distributed to the affected VDCs and Municipalities for their social development. This is adequate amount of money for minimum development of local bodies. However, after the stoppage of extraction of raw materials from the river basin, local bodies have got economic losses.

Though there are direct benefits from the extraction of riverbed materials, in the long run it changes the bed and width of the river and also hampers the structures built across the river and on the banks [18, 19]. Similarly, excessive extraction of riverbed materials from the bed, banks and floodplain areas lowers the ground water table of shallow aquifers and affects the livelihood of the fishers [3,9,20].

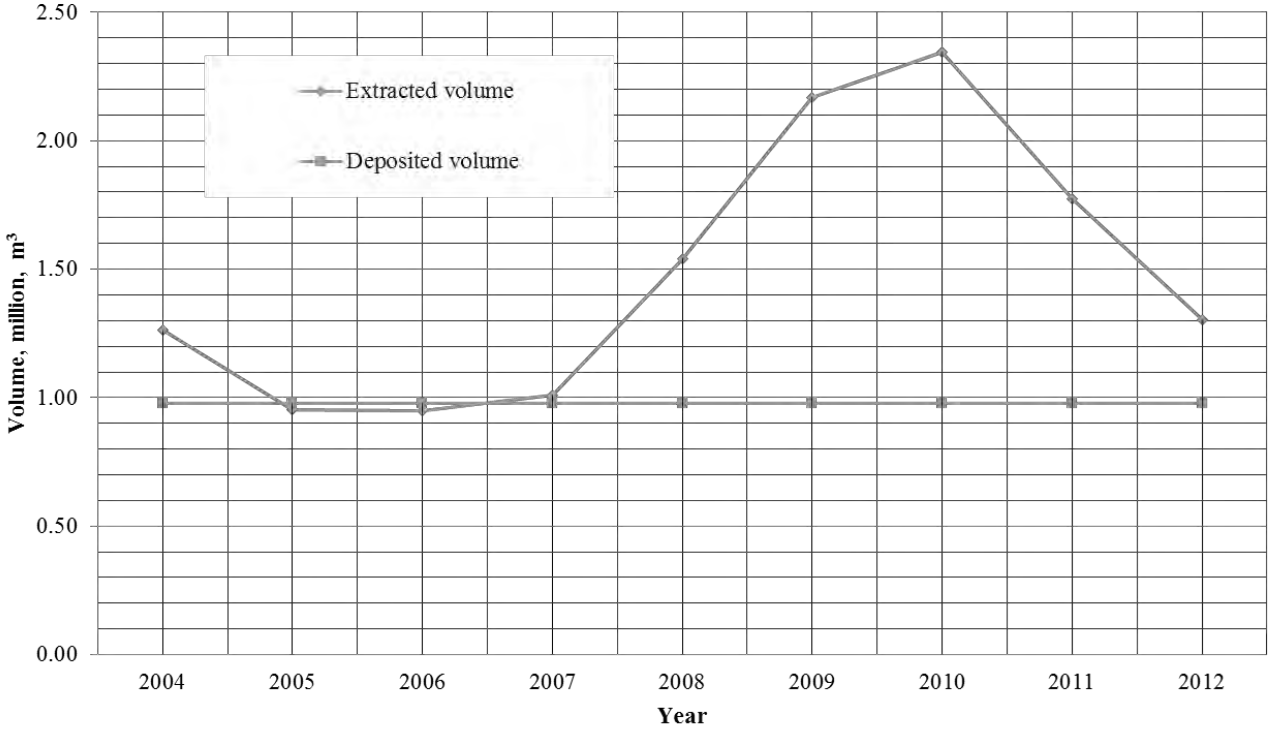

Fig. 3: Extracted and deposited volume of riverbed materials [9]

Riverbed extraction in Tinau River basin is associated with many direct and indirect businesses. Direct businesses are hotels and groceries. Indirect businesses are the employment generation in the extraction work, hotels, industries and groceries. Hundreds of labors (married, unmarried, under aged, over aged) are engaged in the work and they have earned thousands of rupees. Furthermore, such activities have stopped people from searching foreign employment. However, in these days, there are fewer materials and not all factories are working to provide adequate jobs for the locals. During survey at site, many old people living at that locality reported that the extraction of construction materials is beneficial and easy earning source. However, the Supreme Court has decided to extract the materials in certain points, where DDC has

permitted [21]. Experts of this sector feel it as an unnecessary decision. The matter is very controversial and it needs further scientific proofs and investigations.

As the river has incised, there is a need of construction of bed bar throughout the length of Tinau River for stoppage of further degradation [22, 23]. Some social and environmental activists are claiming that crusher industrialists have created danger in Tinau River but, there is no sufficient evidence to support this statement [24]. However, the proper management and regular monitoring of river is lacking. Most of those people are not analyzing the economic return from the riverbed materials; instead talking only about the degradation of environment. Of course, degradation of river environment is a considerable factor but the cost could be internalized in the project [25]. However, this matter has not been considered while awarding contracts of riverbed extraction.

The Constitution Assembly (CA) Committee has also mandated the DDCs to carry out Initial Environmental Examinations (IEEs) or Environmental Impact Assessments (EIAs), of the source rivers and the preparation of environment management plans based on the IEE/EIA findings before domestic tax farming contracts or export permits can be issued [9]. Most districts engaged in river bed materials contracts for domestic sales or export has prepared their IEE/EIAs. The study found that the district IEE/EIA reports followed standard environmental guidelines but differed in content and in their degree of comprehensiveness. In general, the IEE studies that were outsourced to private consultants were more thorough than those carried out by the DDC's own technical staff [26].

Though the riverbed materials are very much useful raw materials for industrialists, there is no analysis on the negative impacts or negative externalities. Furthermore, it affects negatively the base of the infrastructures and damages [9, 20, 23, 27, 28]. The damaged infrastructures should be rebuilt. However, it raises the external cost too.

The total revenue from the riverbed materials in the fiscal year (2009/10) was 1 billion, whereas the repair and maintenance cost of the road was 11 billion [17]. However, extraction of riverbed materials is the major source of livelihood for the poor people in Nepal as well in the countries having low income [29].

Riverbed materials are the backbone of construction industries and are being used in many ways in the world. In some countries, the government has failed to stop the illegal extraction of sand and gravels [9].

In the case of Tinau River, there is a fractured institution. Along the basin there is no implementation of integrated water management. The legal framework is also not working efficiently and effectively [30]. Thus, the river basin itself needs to develop in an integrated approach. Many rivers have the potential for riverbed materials and they can generate millions of Nepalese Currency (NRs/Rs.) if we develop them in a scientific way. During last year, the studied VDCs collected about 4 million cubic feet of riverbed materials from the Tinau River and the revenue they collected was Rs. 11.92 million (Nepalese currency). Similarly, total labors engaged were 1.9 million man days (MD) during the year 2012 to 2013 [26]. However, the planning and proper implementation is lacking [9]. It needs a detailed technical report for monitoring during excavation and extraction of construction materials [31].

4. CONCLUSION

Extraction of riverbed materials creates employment, generates revenues and makes social development of local administrative bodies such as VDCs, Municipalities and DDCs. Local administrative bodies collected 137 million of Nepalese Rupees during last 5 years. Similarly, dozens of labors have got employment and some new businesses such as hotel and small scale groceries have emerged along the bank of Tinau River. Since the materials are in decreasing trend in the river due to over extraction, government has stopped some ports of entries and income generation has decreased. As a result, crusher industries have faced crisis in materials. Some of the crusher plants have already stopped due to lack of raw materials. Local bodies have done many social, educational and infrastructure development with the income from the riverbed materials. However, there was deficit of riverbed materials as the extraction rate was greater than the deposition rate.

5. ACKNOWLEDGEMENT

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AN EMBEDDED SYSTEM FOR SECURE HARDWARE BOOT METHODS

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ABSTRACT

With fabless integrated circuit (IC) design companies growing as the major source of semiconductor designs, and since a multitude of companies can be involved throughout the manufacturing process, many different security issues regarding intellectual property (IP) arise. Some of these hardware security threats include unlicensed overproduction of ICs, or a manufacturer falsely reporting working products as defects, both so that an unauthorized third party may sell the extra goods. The proposed design applies various actively researched technologies in hardware security, as well as includes additional mechanisms to further protect an intellectual property (IP) developer from potentially untrustworthy actions that could occur at a fabrication facility (fab), or within the hands of other various third parties. A primary application, which the innovative portion of this design could protect against, is the scenario where a fab overproduces/clones the IP of a fabless design company, and sells the extra components on the market. Additionally, this innovative feature utilizes technology which can also protect against recycled and out-of-spec components making their way back into the market.

Keywords—*Hardware Security, Hash, LFSR, PUF, Ring Oscillator PUF, Pseudo Random Number Generator*

1. INTRODUCTION

There is a growing concern of recycled, counterfeit, cloned and insecure ICs finding their way into semiconductor market. This growing threat can not only damage a company's profitability, but also can put end-users in danger. The proposed design prevents some of the threats by implementing a simple, yet robust hardware solution that serves as a security mechanism for integrated circuits and embedded systems. The major building blocks of the design include a highly randomized random number generator (RNG), an MD5 hash encryption scheme, an initialization state machine (ISM) and some external control logic such as firmware. These portions of the design are incorporated to create a secure boot method for embedded systems, where a unique key is generated for each piece of hardware that must be provided by external logic to the ISM in order for the system to boot up properly

2. DESIGN OVERVIEW

The motivation behind this design was to create a robust, simple and efficient way to enable an IC designer to protect a fabricated chip from entering the market without permission.

Figure 1 shows a simplified, top level architectural view of the proposed system.

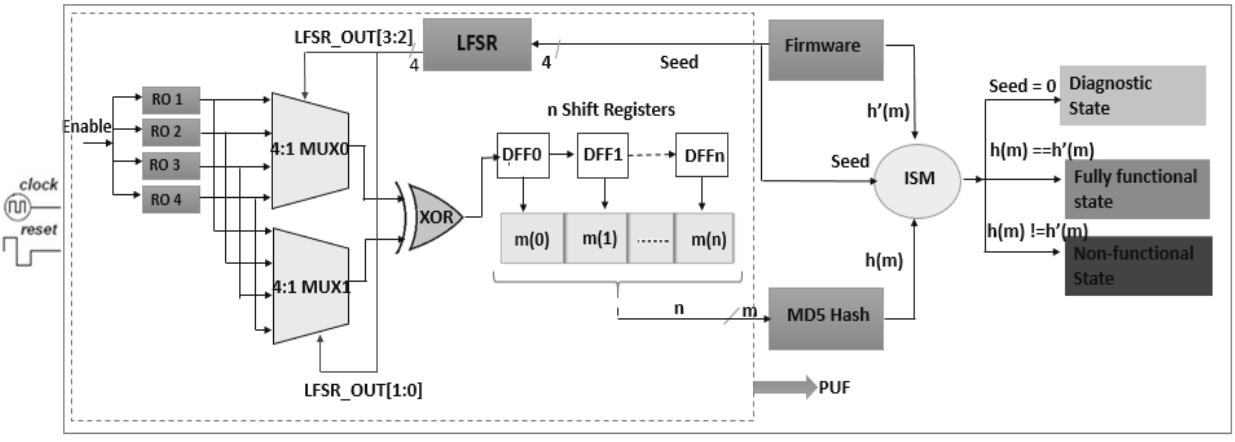

Figure 1 Simplified architectural view of the proposed design

The main modules of the design include a set of four Ring-Oscillators (ROs) with a Linear-Feedback Shift Register (LFSR) to be used as a random number generator, an MD5 hash block, an initialization state machine and some external logic handler – implemented and shown here as modeled firmware. The nature of the RO and LFSR combination classifies it as a Physical Unclonable Function (PUF) [1] which provides a highly unique signature on each IC, and is partially configurable via external inputs. Upon start-up, the firmware would have to provide the proper seed to the LFSR in order to enable the PUF to generate a random message to be sent through the hash block. This encrypted message would then serve as a key to the ISM. The system would then remain nonfunctional until the external logic (firmware) provides the same key value to the ISM. The unencrypted message coming from the PUF is provided to the firmware, where the message must be properly hashed, and then sent to the ISM for the system to become functional. Using the example of firmware, it would be required that the fully functioning firmware not be uploaded/embedded in the device at the time of fabrication. The IC designer or a trusted third party would update the firmware to fully unlock functionality of the system, thus ensuring a secure manufacturing process. In order for the chip to be tested for functionality at the fab, a diagnostic state can be entered by default when the seed value is zero, thus providing some partial functionality for diagnostic purposes.

Essentially, security is a cat and mouse game, where there is always some vulnerability to the system. The whole idea here is that the inner workings are obfuscated enough to cause the tampering of this system to be highly improbable within the devices' critical lifespan in the market. Additionally, the dynamic ability to configure the PUF and allow for different keys to be produced provides further obfuscation and security. The external logic could be implemented however an IC designer sees fit, but modeled firmware was chosen for the external logic handler here since there are multiple methods available for secure firmware uploading on a device [2].

3. PUF DESIGN

1.1. TOP-LEVEL DESCRIPTION. Although all the ICs of same configurations are created using same manufacturing processes, there exist some minute, almost negligible process variations within the designs. The RO PUF takes advantage of those process variations to create a highly unique signature on an IC. By attempting to model four identical paths to the shown multiplexers (MUXs) in *Figure 2*, the minute process variations that occur in the paths and RO frequencies will cause the output of the XOR gate for a given set of MUX select bits (aka challenge) to be highly unique. We use these characteristics of the RO PUF to generate a highly-random sequence 'm', which is very unique to each individual IC. *Figure 2* shows the simplified architecture of PUF. Unique to this design is the control method for the MUX challenge bits. By utilizing some external logic to set the seed of the LFSR, the output of the PUF can be partially configurable and updated overtime. It should be noted that a static challenge can provide an output from the PUF that could be used as part of a serial number for the IC.

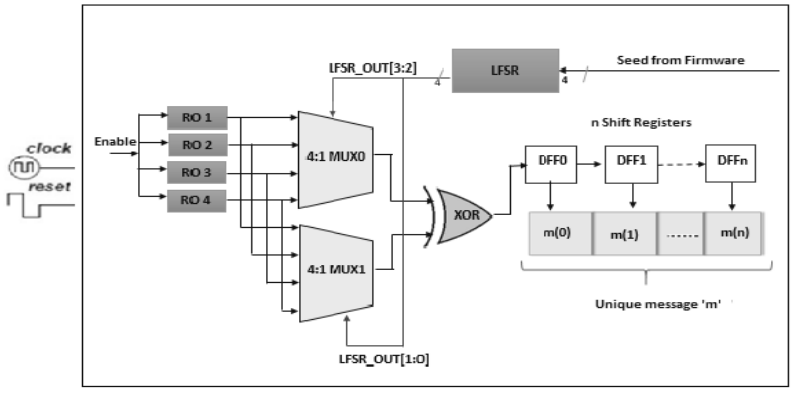

Figure 2 — Simplified view of RO PUF

1.2. LINEAR-FEEDBACK SHIFT REGISTER IMPLEMENTATION A linear-feedback shift register is a regular shift register with two or more register outputs being fed back to the input of a register through an XOR gate [3] as shown in *Figure 3*. The design of a 4-bit LFSR is show below where the output of three registers is fed back to the input through xor gate.

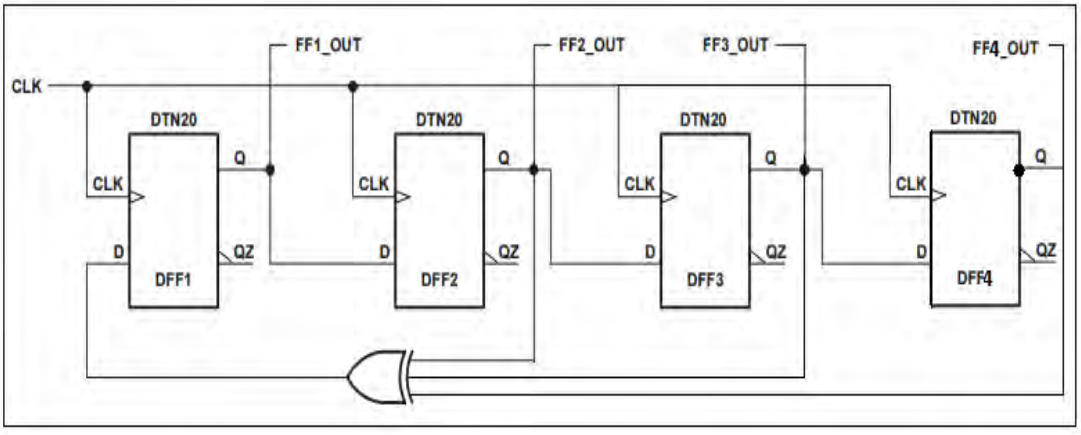

Figure 3 - 4-bit Linear Feedback Shift Register

Upon receiving a non-zero seed at FF*x*_OUT, pseudo random bits are seen as outputs starting the next clock cycle. While the seed is zero, the output of the LFSR remains zero. The reason behind calling the sequence pseudo random is for a given seed, the sequence of outputs at consecutive clock cycles is the same. Also, for an n-bit LFSR, the sequence repeats itself after 2^n clock cycles.

For our design, we used the LFSR to generate a 4 bit pseudo random number which is used as selections bits for the multiplexers. These selection bits enable the multiplexers to choose randomly from the available RO outputs. By utilizing the characteristic of an LFSR statically outputting zeros when a zero seed is given, we can allow the system to enter a semi-functional state where basic testing or further diagnostics can take place.

1.3. ROS WITH SHIFT REGISTER The RO PUF integrated here was reviewed to be one of the more advanced, successfully implemented methods [4] and borrows ideas discussed by *A. Maiti et. al.* [5] that addresses some issues regarding metastability and narrow pulse rejection attenuation of high frequency components an XOR tree by adding extra sampling flops on the RO outputs in order to hold the outputs stable for one whole clock (shown in *Figure 4*).

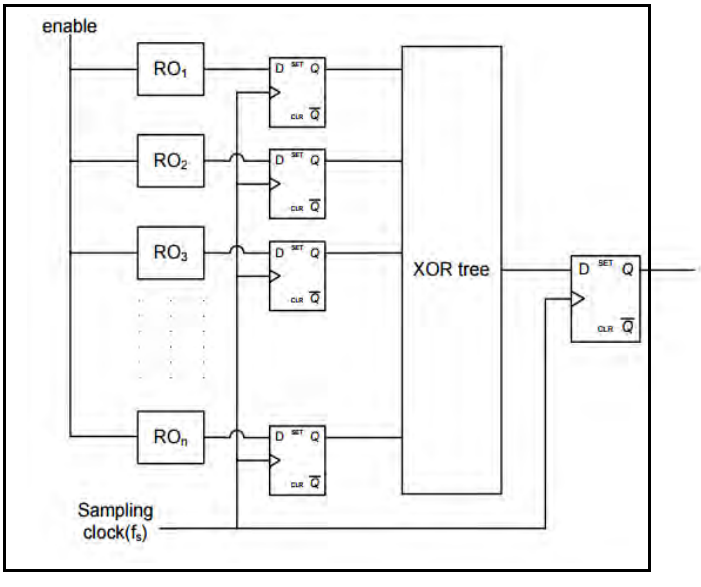

Figure 4 — Stable sampling of RO outputs [5]

This concept was introduced into our design by adding flops to the ROs prior to entering the multiplexers. Only a single XOR was used here since the approach of using MUXs only provides two outputs to consider, rather than a comparator presented by *A. Maiti et. al.* [5].

From here, the Verilog code was written for the shift register to be parameterisable, and able to shift out 'n' bits prior to turning off the PUF and sending the message off to the hash block. The max length allowed by the PUF output would be 128 bits, since that is the length limitation for the MD5 hash used. It should be noted that the higher the number of ROs used, the higher the max entropy of the PUF output [6].

4. MD5 HASH

The hash used here was developed by *S. Mitra et. al.* from MIT, and is publicly available through the GNU license [7]. The motivation of encrypting the message using a hash was to provide further obfuscation by generating a new key from the randomly generated PUF output. This is useful since it requires the external logic (firmware) to have knowledge of the design in order to accurately generate the same key using the PUF output. Additionally, an MD5 hash is generally lightweight, and can generate an output fairly quickly when compared to other encryption schemes. Although the MD5 hash has come under recent scrutiny for possible collisions [8] where the properties of a hash being a one way function are violated, the use of an MD5 hash in key creation should still provide enough diversion to serve the purpose of the system.

5. ISM

The initialization state machine is responsible for setting the device into three possible states after coming out of reset – diagnostic or semi-functional state, fully functional state and non-functional state. *Figure 4* shows a simplified view of the ISM flow.

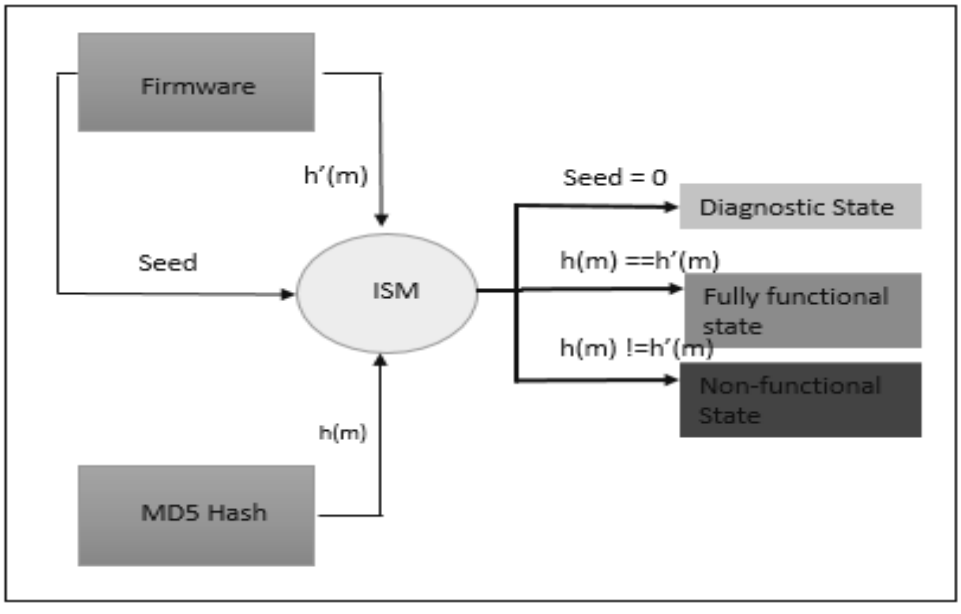

Figure 5 -- ISM Behavioral Schematic

DIAGNOSTIC OR SEMI-FUNCTIONAL STATE As previously discussed, as long as the seed provided to LFSR is zero, the output remains zero. When providing IP to the fab, the default value of the LFSR seed should always be zero. This enables the fabrication facility to test the basic functionalities of the IC without knowing the key to access the secured functions of the system. These secured blocks within an IC can only be unlocked by the IP designer by providing a non-zero to the LFSR, thus generating a random message from the PUF so that the hash key can be calculated.

FULLY FUNCTIONAL STATE When manufactured ICs are received by the IP design company, the designer will upload a non-zero seed to the LFSR through the firmware. This will result in the generation of pseudo random sequences for every clock cycle. The generated hash function h'(m) is stored to be used later at the consumer end. When a consumer turns on the device with our embedded hardware security boot block, another hash function h(m) is calculated in real-time and compared with the stored hash function h'(m). Only when these two values are equal the system enters fully functional state.

NON-FUNCTIONAL STATE In our design we use Physically Unclonable Function (PUF) to generate the random message m which is then hashed to produce hash function h(m). Any slight tampering with the device would change the message m. Any minute change in m would result in h(m) which will be drastically different from the stored h'(m). When h (m) is not equal to h'(m) the device is set in Non-functional state.

6. CONCLUSION

The proposed system serves as an initial proof of concept to how an IC designer could use RO PUFs, a basic hash encryption scheme, and a simple ISM in order to obfuscate functionality of a system in a way that provides means for a secure boot method. The external logic that handles the calculation of the expected hash key generated, as well as configuring the PUF to act as a RNG, provides an IC designer flexibility in choosing what piece of logic should interface with the secure boot embedded system. Furthermore, by allowing the system to have a partially functional "diagnostic state", a fab is still capable of performing basic testing of the manufactured IC without having the external logic (potentially firmware) present or fully functional on the device at the time of fabrication.

7. FUTURE RESEARCH

A further research is being done to further obfuscate the security details in an embedded system. One possible way of achieving this is by altering the process of generating hash function h(m). There are initial states in MD5 Hash which are further processed, along with the provided input message m, to generate a hash function h(m). We are studying further to see the effect of changing these initial state values with respect to the LFSR_OUT received from the Linear Feedback Shift Register (LFSR). Another possibility of increasing the obfuscation levels that we are studying is to select only certain bits of message m generated by PUF instead of the whole message m. On doing this it is expected that the uniqueness of keys generated by the proposed secured boot method will be increased.

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PERFORMANCE AND TIMING ANALYSIS OF ARM CORTEX PROCESSORS USING IN-ORDER AND OUT-OF-ORDER EXECUTIONS

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ABSTRACT

From the past, ARM processors had been famous in their simpler architecture design using RISC and the lower power consumption comparing to Intel processors. This paper presents the In-order execution and out-of-order execution in ARM processors. In this paper two different ARM cortex processors are used, and their performance and timing was analyzed. For In-order execution ARM Cortex A8 processor was considered and for out-of-order execution ARM cortex A9 processor was considered. A new application has been designed here with the help of JAVA programming, to show the performance analyses in ARM cortex A8 and ARM cortex A9 processors and named it as "Performance Analyzer". To show the timing analyses between this processors an application known as "Assembly Emulator" has been used.

Keywords— *Another machine, activities and services, CSV files, graphic user interface, virtual machine.*

1. INTRODUCTION

In In-order execution the instructions are fetched, executed and completed in compiler generated order. If input operands are available (in registers for instance), the instruction is dispatched to the appropriate functional unit. If one or more operands are unavailable during the current clock cycle (generally because they are being fetched from memory), the processor stalls until they are available. In in-order execution instructions are statically scheduled. In out-of-order execution it allows the processor to avoid a class of stalls, which occur when the data needed to perform an operation that are unavailable. In the outline, the out-of-order execution processor avoids the stall when the instruction is not completely ready to be processed due to missing data. In-order execution does not always give the best performance on superscalar machines. The two major factors for using in-order execution was it requires low power and it has low complexity architecture. Where as in out-of-order execution it requires high power and the architecture is more complex, but it would speed up the performance in return. Things have been changed over the years; ARM has grown more complex instruction set computing, while Intel has become streamlined in other areas. In this paper we have designed an application "Performance analyzer" to calculate the performance of the ARM processors. With the help of this performance analyzer we have calculated the usage of Memory, buffers, CPU etc. and we have shown them in graphic form where we can record, pause and save the graphs. To investigate the timing analyses among the ARM Processors, a nested loop program is considered.

2. BASIC CONCEPT OF IN-ORDER AND OUT-OF-ORDER EXECUTION

In a dispatch, instructions are sent to a functional unit. The dispatch of instructions is shown in Figure 1.

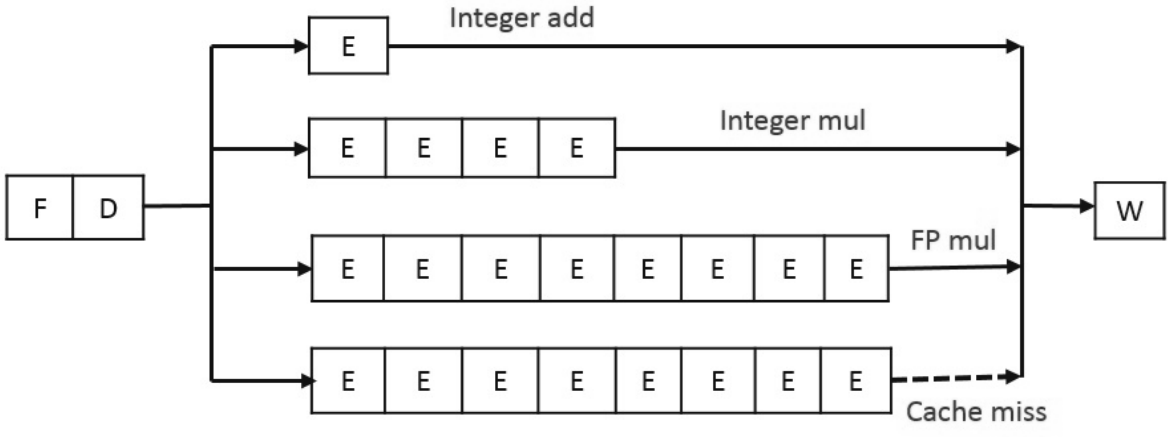

Fig. 1 Dispatch of instructions

The process consists of four stages of instruction dispatch. They are fetch (F), decode (D), execute (E) and write (W). Let's take an example to explain this. Let's say that C is equal to A into B, and D is equal to the addition of C and E. And F is equal to the addition of G and H. While executing this example in In-order execution, the entire pipeline will be stalled. D cannot dispatch because one of its output variable is dependent on C. Until the dispatch of C is completed we cannot execute the next stage, which leads to stall in the In-order execution. C has to perform multiplication operation which takes more time than addition, so until the result of C is executed D cannot complete the execution, which leads to delay. Therefore, the independent instruction F cannot be executed. So the entire In-order execution pipeline will be stalled as shown in figure 2.

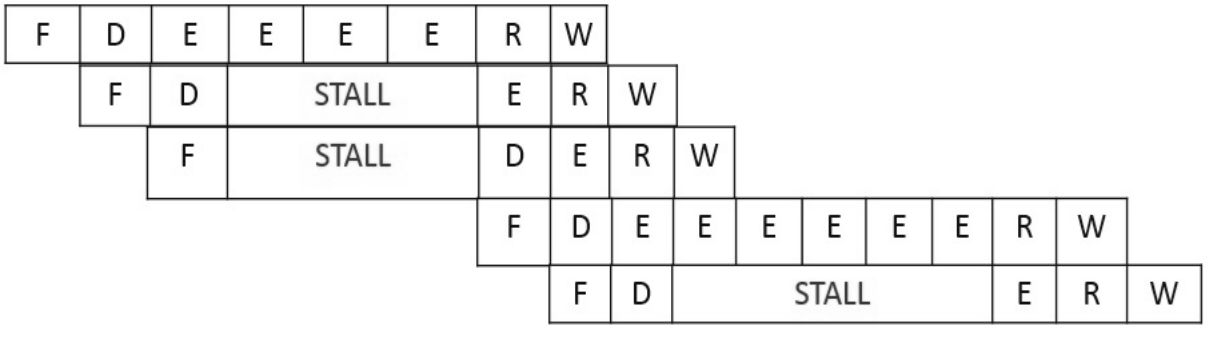

Fig. 2 In-order Dispatch

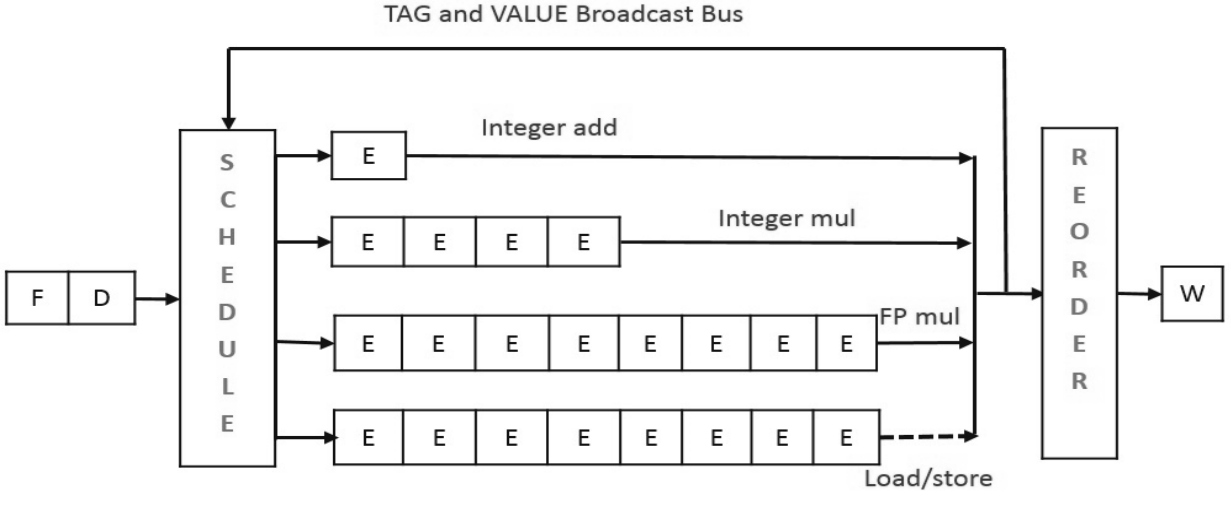

Fig. 3 Out-of-order Dispatch

To overcome the stall that occurs in In-order execution, we move to out-of-order execution. In out-of-order execution the independent instructions are executed first and later dependent instructions are executed. In out-of-order execution the instructions are fetched, and then the instruction is dispatched to an instruction queue. Until its input operands are available the instruction waits in the queue and the instruction is then allowed to leave the queue before earlier, older instructions. The instruction is executed by that unit and is issued to the appropriate functional unit, hence the results are queued. This result is written back to the register file, only after all older instructions have their results written back to the register file. Due to this concept, out-of-order execution processing allows the processor to avoid a class of stalls, which occur when the data needed to perform an operation are unavailable. When the instruction is not completely ready to be processed due to missing data, the out-of-order execution processor avoids the stall unlike the stalls that occur in the in-order execution processor. If we consider the same example which is used for In-order execution the instruction F will be executed first because it is an independent instruction. The D and C instructions are also executed even though they are dependent instructions. In a processor, avoiding a class of stalls will leads to time consuming.

3. TIMING ANALYSIS

For calculating the timing analysis between In-order execution and out-of-order executions we consider the processors ARM cortex A8 and A9 processors. ARM cortex A8 processor uses In-order execution and ARM cortex A9 processor uses out-of-order execution. In this work we have chosen two mobile phones in which one mobile phone has ARM cortex A8 processor in it and other phone which has ARM cortex A9 processor. SO this whole experiment will be carried through two mobile phones. For calculating the timing analysis on A8 and A9 processors we have considered a nested loop program. Because, if the program that is under execution has a data dependency then Out of Order Execution executes faster than In-order execution. Therefore, we have chosen a program with data dependency and executed in both the processors. The time taken for the execution has been recorded with the help of Assembly Emulator in Android.

```
#2 nested loops
#useful for determining execution speed
addi $s2, $zero, 3000        #repeat loops for k times
first loop:
addi $s1, $zero, 1           #i = 1
second loop:
addi $s1, $s1, 1             #i = i + 1
bne $s1, $s2, second loop    #if i is not equal to k go to second loop
addi $s3, $s3, 1             #j = j + 1
bne $s3, $s2, first loop     #if j is not equal to k go to first loop
```

When we run this program in both the environments of ARM Cortex A8 and A9, the timing analysis is predicted. Timing analysis is a method to analyze time between two parts. Here we are analyzing time difference between ARM cortex A8 and ARM cortex A9 by using ASSEMBLY EMULATOR application.

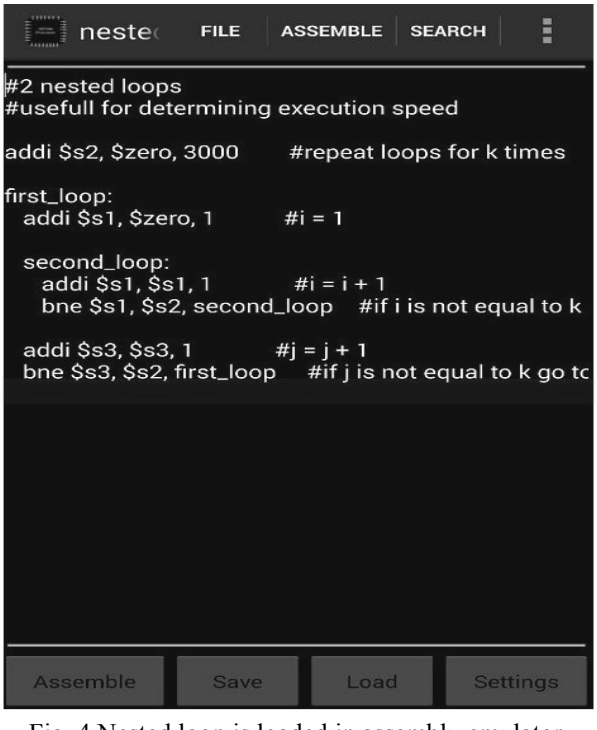

Fig. 4 Nested loop is loaded in assembly emulator

In the assembly emulator, the code which is a nested loop is loaded as shown in figure 4.After assembling the code a window will be shown in which we can see number of processed lines of code in milliseconds as shown in figure 5.

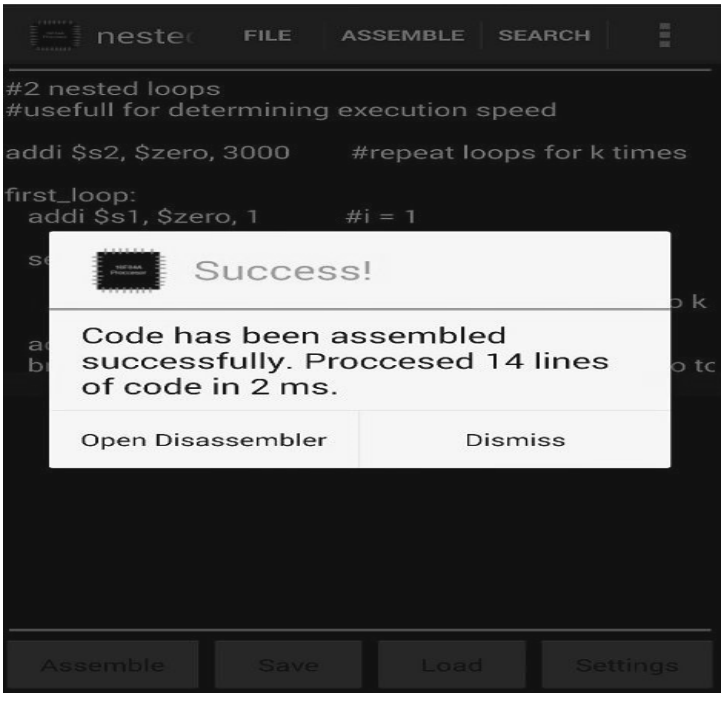

Fig. 5 Assembling code

When clicking the open disassembler we can see the assembling code and registers allotted. Soon after executing the code we can see total number of instructions executed and total time taken. Figure 6 shows the total number of instructions executed for the total time taken for ARM cortex A8 processor.

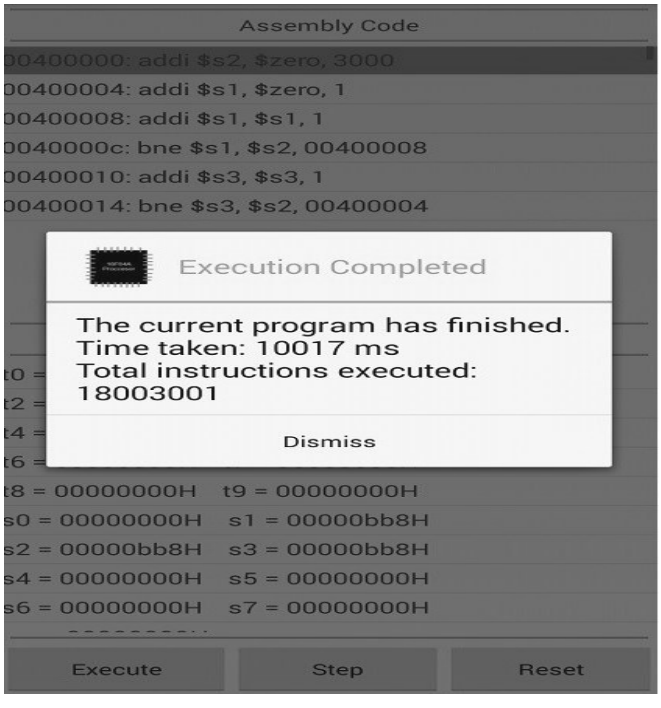

Fig. 6 Execution of Cortex A8 Processor

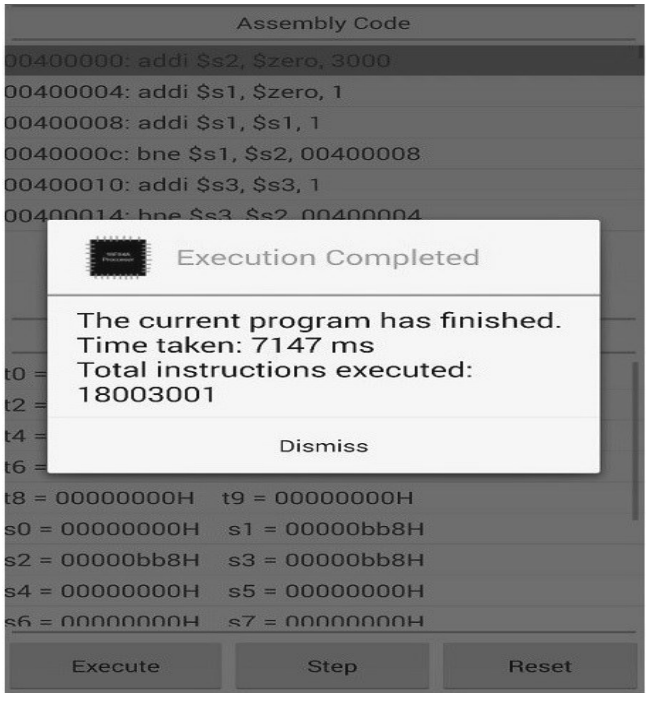

Fig. 7 Execution of Cortex A9 processor

In the ARM cortex A9 processor, the total number of instructions executed for the total time taken is shown in figure 7. In the figure 6 it is shown that the time taken by ARM cortex A8 processor to complete 18003001 instructions is 10017ms. Also in the figure 7 it is shown that the time taken by ARM cortex A9 processor to complete 18003001 instructions is 7147ms.

Considering the executions of the ARM cortex A8 and A9 processor, it is clearly seen that ARM cortex A9 processor executes total number of instructions in less time than comparing to A8 processor. Therefore, we can say that ARM cortex A9 processor which is using out-of-order execution is a time-consuming system. The cortex A9 processor

achieves a better than 50% performance over the cortex A8 processor in a single core configuration. The graphical representation is shown in figure 8.

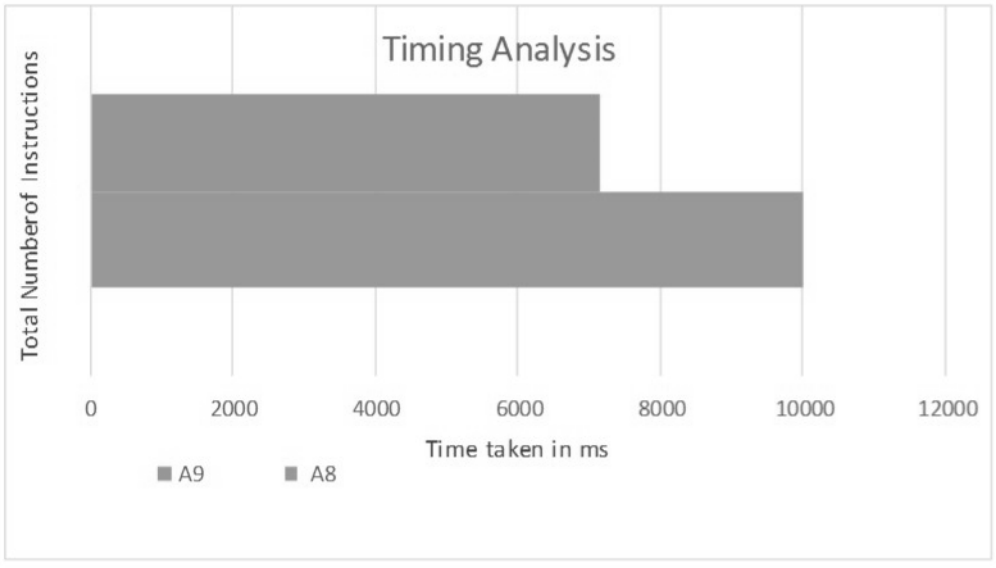

Fig. 8 Timing analysis in Arm cortex A8 and A9 processors

4. PERFORMANCE ANALYZER

Performance Analyzer is an application which we have designed for the Android platform. This application monitors and records the memory and CPU usage values of the processors. This application can be installed efficiently to any mobile phones, tablets and laptops, to know the processors resources state. Performance analyzer has 2 main features - a graphic and CSV file. In graphic class the values of the memory and CPU usage will be updated in real time and the values will be shown in graphical form. The CSV files record the values that are updated in graphic class and stored in a spreadsheet program for future usage. The program can be executed in background. Since the program can be run in background, performance Analyzer consumes little resources to monitor and record the memory and CPU usage values.
As mentioned earlier, in this work we have chosen two mobile phones with A8 and A9 processor. To this two mobile phones we have installed the performance analyzer.

4.1 TECHNICAL DETAILS: Performance Analyzer application has been developed by using JAVA with the Eclipse IDE and ADT plugin. The minimum requirement for this application is a compatible device with Android 1.5 or higher. The performance analyzer has been tested successfully up to Android 2.2. Version. The application uses the architecture components of the android platform which we named them as “Activities and Services”.

In Android, the activities are the visible part of the program .The activities show the information and interacts with the user through graphical icons and visual indicators which is known as “Graphical User Interface (GUI)”. In another hand, services are usually the part of the program which has no need to interact with the user and it has no GUI and often runs repetitive tasks.

Performance Analyzer performs three activities which means one activity for each window. The three activities are: The main activity, The Preferences activity and The About activity. The most important activity is the main activity. The main activity is the first code of all the program what Dalvik Virtual machine runs. It shows (but does not make) the graphic and the text labels, it starts the service and manage another minor task like the main menu. The Preferences activity opens a new window where the user can configure several parameters of the program. The About activity shows a window where information about Performance Analyzer appears.

By user indication, the service will proceed to read and record the values of the memory and CPU usage every time interval (by default, 1 second) in a CSV file. The CSV files can be used for future referral purpose. These CSV files are saved in the mobile in the folder data/data/com.anothermonitor/files. Later, these values are used by the main activity to show them to the user. Every time we perform an activity the service class reads and records the values. When the main activity is performed the service class will receive a code, which is executed by a virtual machine. After receiving a code from main activity, the service class uses the code to show the graphic and text labels of the main menu. In this main menu we can see the memory and CPU usage values.

4.2 PROGRAM PERFORMANCE: Since the program scope is to monitor the memory and CPU usage, the performance analyzer consumes little resources which is a fundamental. Unfortunately, this premise is not always carried out by Performance Analyzer. The performance of the application is different depending in what mode it is. Of course the power of the mobile also plays a vital role. In the beginning to show the graphic, memory CPU usage values it uses around 40-70% of

the resources, but this percentage may vary depending on Read, Draw and Width intervals. The lower parameters, the lower CPU usage. We can choose different configurations which are required anytime. On another note, if Performance Analyzer is reading values in the background, the CPU usage is low which depends on the read interval. But generally it is around 5-10%. If the application is still recording the usage does not increase.

In the foreground mode, the code that is recursively running is a new thread in an AnReaderService instance which is reading values, and a runnable in the main application thread updating the lifelike. This runnable updates every interval of time all the text labels and call to the invalidate() inherited method of the AnGraphic instance (which call to onDraw() to redraw newly all the whole graphic. Although it follows the recommended implementation to update views and layouts, this operation consume quite resources. Besides, if the application is in the background mode, the one running code is the reading thread which call to the method read() to access the memory and CPU statics of the Linux mobile machine. This operation consume little resources.

4.3 GUI AND DIFFERENT SCREEN RESOLUTIONS: Performance Analyzer support all possible resolutions of the Android platform, from 320x240 up to 1920x1080. If in the future the Android platform supports more new high resolutions, the current version of Performance Analyzer will not have problems to manage them. The main window has a portrait and a landscape version. The landscape version changes the screen scheme from up-down to left-right. To fit to small-LDPI screens in landscape mode there is another specific version. In total there are three different main.xml files.

4.4 PROGRAM STRUCTURE

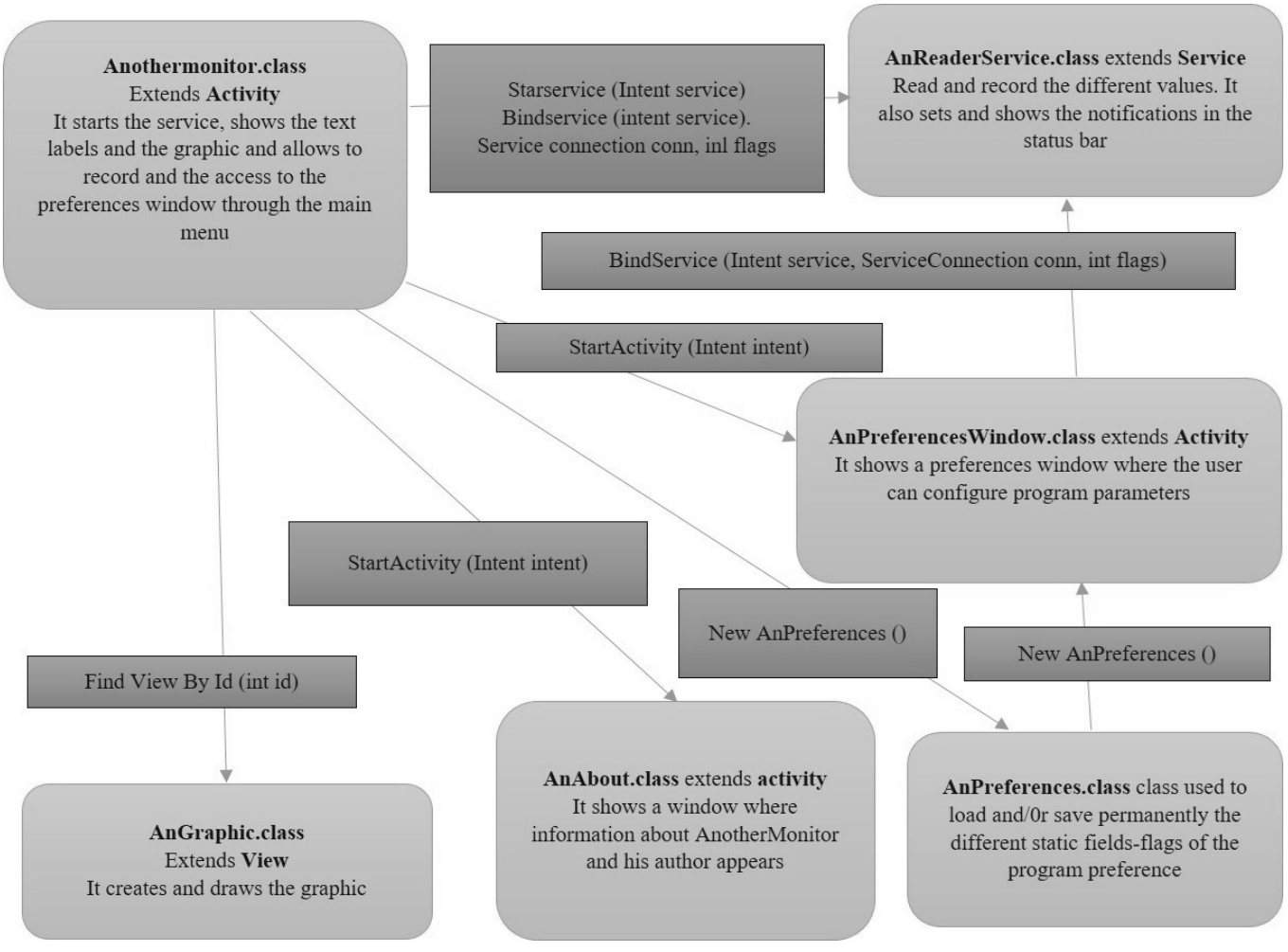

Fig. 9 Program Structure of Performance analyzer

4.4.1. ANOTHER MONITOR. CLASS: It is the main activity and the first run code of all the program. In this we use onCreate() method which starts the service and loads the GUI from the main.xml file. This onCreate() method loads or create the preferences. As soon as the bind between the activity and the services is created the interface mConnection() will be called. This implemented interface pass the vectors of each read value of AnReaderService class to AnGraphic class and starts to run the runnable draw Runnable(). This Runnable() updates repetitively every time interval of the text labels and the graphic. Another important feature of Performance Analyzer class is the management of the main menu:

onCreateOptionsMenu (), onPrepareOptionsMenu (), and setMenuIcons ().

The onCreateOptionsMenu () loads the menu from the menu.xml file and check it with the flag

myAnReaderService. In this main menu we can see the record icon. We can record the graph. While the graph is being recorded we can use another activities. While using other activities there is a chance that the previous activity which is running in the background has to be relaunched, because of the lack of memory. In such cases it stops recording and saves until what we recoded till the end. This way the recording can be saved without being erased. The onPrepareOptionsMenu () and setMenuIcons () methods are used to check and change the appearance of the menu icons between the NORMAL icons and the HAPPY ones. Figure 10. shows that menu icons where we can record, pause and choose preferences.

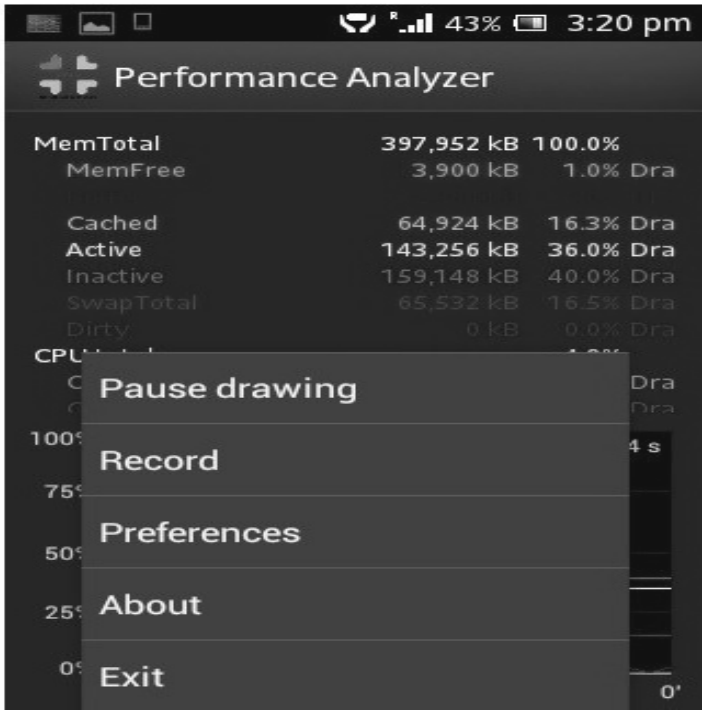

Fig. 10 Performance analyzer menu window

4.4.2. AnReaderService.class: The main scope of this class is to run a service. AnReaderService.class reads and (if selected) records the memory and CPU values of the mobile Linux system as shown in Figure 11.The onCreate () method creates the vector for every value and shows the Android status bar notifications.

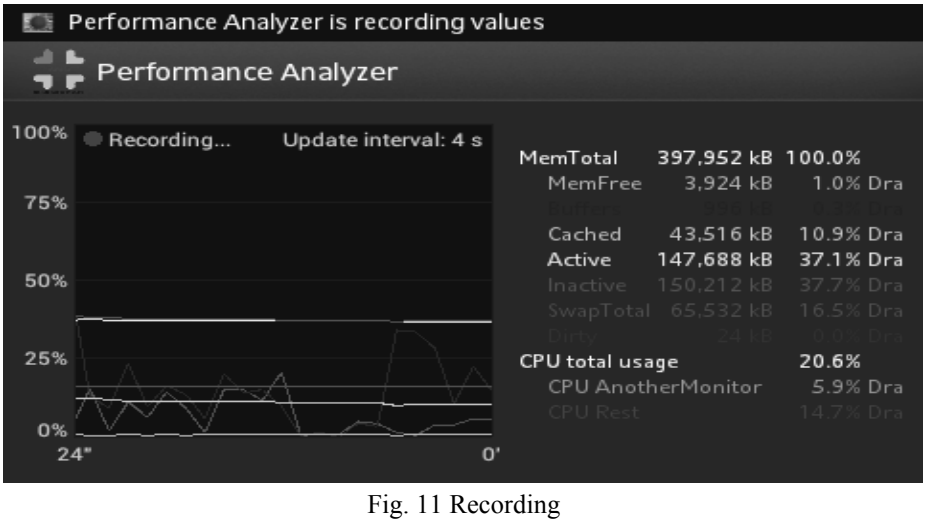

Fig. 11 Recording

The view AnGraphic does not connect directly to the service because, it extends View. The AnGraphic class creates and draws the graphic. The data structure selected to keep the values is a 'vector' (implemented in Java by the class Vector) in place of another like queues. Because the class Vector is the one that allows to see, modify or remove any element of the structure without the need of that element in the first position. To read the values, the onCreate () method is created and starts a new thread for every time interval that has been called to the read () method. This method reads and saves values, and when the AnReader Service. RECORD flag is executed we can start recording.

The memory values are read directly from the *meminfo* file of the Linux *proc* file system. In another hand, the CPU usage values do not appear in any place. It must be calculated from the values of the *stat* file. It is possible that negative values or values higher than 100% appear. See with more detail how to calculate the CPU usage values (9).The stopRecord () is called when we want to stop a record. The getOutputStreamWriter () and getDate() methods are

exclusively used by record(). This class also helps to show notifications on the status bar.

4.4.3. AnGraphic.class: The AnGraphic class takes care of drawing and updating every time interval in the graph, as shown in figure 11. Using onDraw() method, AnGraphic class helps to draw the graphic lines in the application. This graphic lines indicate the each value of the memory and CPU usage. Here we use drawRect() and drawLine() methods. This methods are useful to draw line to line graphs, grid lines etc. for each value of the memory and CPU. This class helps to change the color of the line and we can select the required parameters easily. We can set the preferences without any disturbance in the activities. This class also consumes few resources, which helps in the performance. Here we use intializeGraphic() program to initialize the parameters of the graphic. This initialization includes color of the line, thickness of the line, shape of the line, curves, etc.

4.4.4 AnPreference.class: AnPreference class has only two methods: readPref () and writePref (). ReadPref () reads (or creates the default values) the memory usage, buffer and cached values that are permanently given to the mobile system. WritePref() modifies and saves the values using AnPreference windows class. This class allows the user to configure few parameters of Performance Analyzer. It is a typical preferences window of any program. The preference activity shows a window with four tabs: Main, Appearance, Read/record and Draw (figure 12, 13).

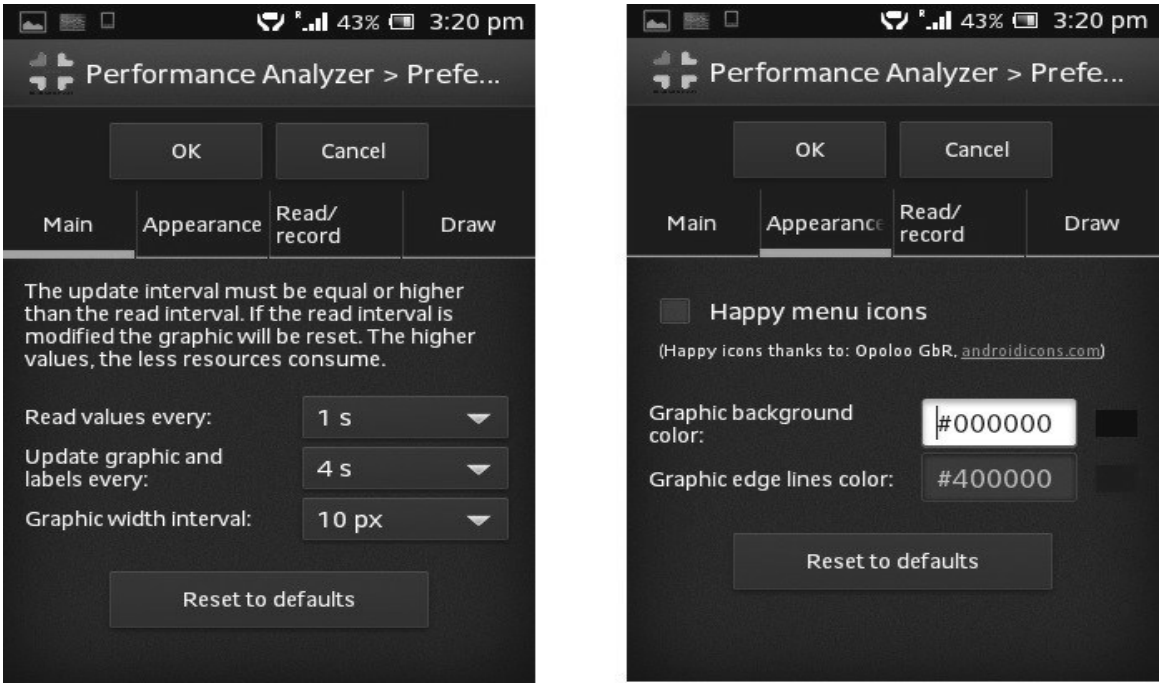

Fig. 12 Main Activity and Appearance activity

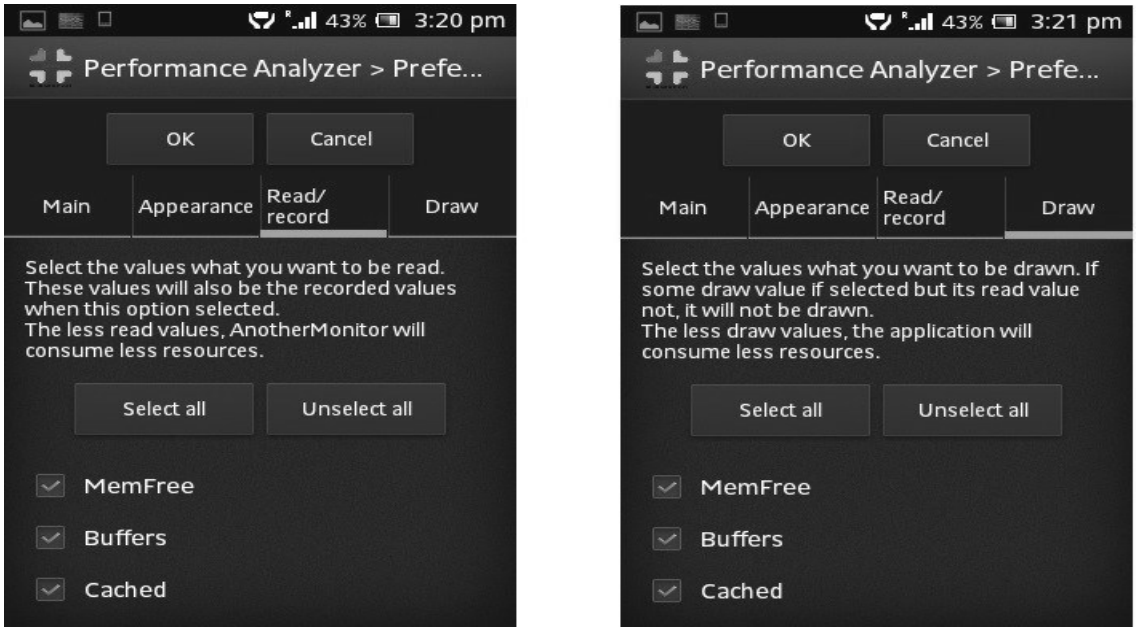

Fig. 13 Read/record activity and Draw activity

4.4.5 AnAbout.class : AnAbout.class is to show the information regarding program and the company. It shows a window with information about the program and the company. The CSV files are saved in the data/data/com.anothermonitor/files folder of the mobile.

4.5 PERFORMANCE OF THE PROCESSORS: Using this application we have calculated and recorded the values of the A8 and A9 processor. After analyzing the performances between the ARM cortex A8 and A9 processors, a graph has been designed. The below graph figure. 14 shows the performance accuracy between the ARM cortex A8 and A9 processor. By this we can say that the ARM cortex A9 processor has better performance than A8 processor.

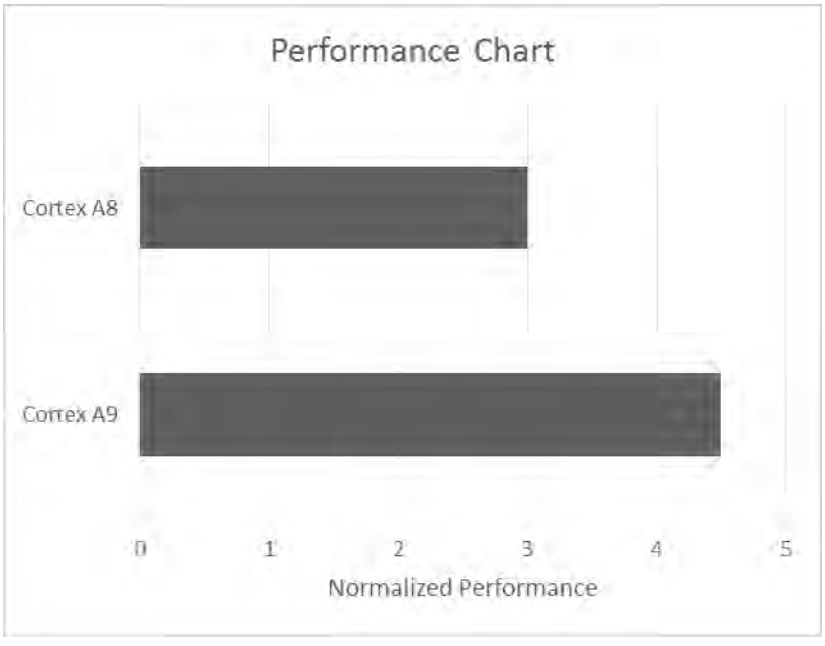

Fig. 14 Performance analysis of A8 and A9 processors.

5. CONCLUSION

It has been shown and verified in our study that the ARM cortex A9 processor with out-of-order execution is more efficient than ARM cortex A8 processor with in-order execution in terms of performance and timing analysis. Overall the ARM cortex A8 processor requires more power and 10017ms to execute the total number of instructions as of the instructions being stalled in the instruction pipeline when compared to the ARM cortex A9 processor that requires less power and less 7147ms to execute the same number of instructions. In the terms of performance from our work we were able to gather that A9 is 30% more efficient than A8 processor. For future work, we plan to extend to verify the timing and performance analyses in ARM cortex A57.

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REDUCTION OF REAL POWER LOSS BY USING ENHANCED ARTIFICIAL BEE COLONY ALGORITHM

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ABSTRACT

In this paper, a new Enhanced Artificial Bee Colony Algorithm (EABCA) is proposed for solving reactive power dispatch problem. Artificial Bee Colony (ABC) algorithm is superior in the exploration part, but it is not well sufficient in the exploitation part. To surmount this problem, instead of arbitrary distribution of the scout bees in the explore space in ABC algorithm, this paper incorporate the Levy Flight in the ABC algorithm and performing the allocation using Levy Flight method. By this way, it was guaranteed that the ABC algorithm has improved the exploitation. The proposed Enhanced Artificial Bee Colony Algorithm (EABCA) has been tested in standard IEEE 30, 57,118 bus test systems and simulation results show clearly the better performance of the proposed algorithm in reducing the real power loss and control variables are well within the limits.

Keywords—*Optimal Reactive* ***Power, Transmission loss, Artificial bee colony, levy flight levy distribution.***

1. INTRODUCTION

The main objective of optimal reactive power dispatch (ORPD) problem is to minimize both the real power loss and bus voltage deviation. Various numerical methods like the gradient method [1-2], Newton method [3] and linear programming [4-7] have been adopted to solve the optimal reactive power dispatch problem. Both the gradient and Newton methods have the complexity in managing inequality constraints. The problem of voltage stability and collapse play a vital role in power system planning and operation [8]. Evolutionary algorithms such as genetic algorithm have been already proposed to solve the reactive power flow problem [9-11]. In [12, 13], Hybrid differential evolution algorithm and Biogeography Based algorithm is projected to solve the reactive power dispatch problem. In [14, 15], an improved fuzzy based method and evolutionary programming is used to solve the optimal reactive power dispatch problem. In [16,17], the optimal reactive power flow problem is solved by integrating a genetic algorithm with a nonlinear interior point method and pattern algorithm is used to solve ac-dc optimal reactive power flow model with the generator capability limits. In [18, 19] a two-step approach and a programming based approach is used to solve the optimal reactive power dispatch problem. In [20] a probabilistic algorithm is utilized for optimal reactive power provision in hybrid electricity markets with uncertain loads. This paper proposes Enhanced Artificial Bee Colony Algorithm (EABCA) for solving reactive power dispatch problem. There are two significant points for biological-inspired algorithms: exploration and exploitation. The exploration part is about the ability of freely seeking for the global optimum, whereas the exploitation part is related to the capability of applying the existing knowledge to look for better solutions [21]. ABC is good in exploration, but it is not good enough in exploitation. The ABC algorithm can execute global search better, it is feeble in local search. In this paper, instead of selecting an arbitrary food source within the search space, it was guaranteed a new food source search be performed according to Levy Flight distribution. Global Min (the food source giving the most excellent result at that time) information

were also utilized while searching for a new-fangled food source with this distribution. Thus, by performing explore around Global Min, it was that the ABC algorithm performs local search more successfully. The proposed algorithm EABCA has been evaluated in standard IEEE 30, 57,118 bus test systems. The simulation results show that our proposed approach outperforms all the entitled reported algorithms in minimization of real power loss.

2. PROBLEM FORMULATION

2.1 ACTIVE POWER LOSS The objective of the reactive power dispatch is to minimize the active power loss in the transmission network, which can be described as follows:

$$F = PL = \sum_{k \in Nbr} g_k \left(V_i^2 + V_j^2 - 2V_iV_jcos\theta_{ij}\right) \quad (1)$$

Or

$$F = PL = \sum_{i \in Ng} P_{gi} - P_d = P_{gslack} + \sum_{i \neq slack}^{Ng} P_{gi} - P_d \quad (2)$$

Where g_k is the conductance of branch between nodes i and j, Nbr is the total number of transmission lines in power systems. P_d is the total active power demand, P_{gi} is the generator active power of unit i, and P_{gsalck} is the generator active power of slack bus.

2.2 VOLTAGE PROFILE IMPROVEMENT For minimizing the voltage deviation in PQ buses, the objective function becomes:

$$F = PL + \omega_v \times VD \quad (3)$$

Where ω_v: is a weighting factor of voltage deviation.
VD is the voltage deviation given by:

$$VD = \sum_{i=1}^{Npq} |V_i - 1| \quad (4)$$

2.3 EQUALITY CONSTRAINT The equality constraint of the ORPD problem is represented by the power balance equation, where the total power generation must cover the total power demand and the power losses:

$$P_G = P_D + P_L \quad (5)$$

This equation is solved by running Newton Raphson load flow method, by calculating the active power of slack bus to determine active power loss.

2.4 INEQUALITY CONSTRAINTS The inequality constraints reflect the limits on components in the power system as well as the limits created to ensure system security. Upper and lower bounds on the active power of slack bus, and reactive power of generators:

$$P_{gslack}^{min} \leq P_{gslack} \leq P_{gslack}^{max} \quad (6)$$

$$Q_{gi}^{min} \leq Q_{gi} \leq Q_{gi}^{max}, i \in N_g \quad (7)$$

Upper and lower bounds on the bus voltage magnitudes:

$$V_i^{min} \leq V_i \leq V_i^{max}, i \in N \quad (8)$$

Upper and lower bounds on the transformers tap ratios:

$$T_i^{min} \leq T_i \leq T_i^{max}, i \in N_T \quad (9)$$

Upper and lower bounds on the compensators reactive powers:

$$Q_c^{min} \leq Q_c \leq Q_C^{max}, i \in N_C \quad (10)$$

Where N is the total number of buses, N_T is the total number of Transformers; N_c is the total number of shunt reactive compensators.

3. ARTIFICIAL BEE COLONY (ABC) TECHNIQUE

Artificial Bee Colony (ABC) Algorithm [22] is an optimization algorithm based on the intellectual foraging behavior of honey bee swarm. The colony of artificial bees consists of three classifications : employed bees, onlookers and scouts. An employed bee search the target where the food is available. They accumulate the food and return back to its source and then they carry out waggle dance depending on the amount of food available at the target. The onlooker bee observe the dance and follows employed bee depends on the probability of the available food .if amount of food is very high then more onlooker bees will follow the employed bee . The employed bee whose food source becomes abandoned then it convert into a scout bee and it will search for the fresh food source. In this problem we consider as employed bee searches the solution in the explore space and the value of objective function associated with the solution is the amount of food linked with that solution. Employed bee renew its location using Equation (11) and it renew its new location if it is better than the preceding position.

$$v_{ij} = y_{ij} + R_{ij}(y_{ij} - y_{kj}) \tag{11}$$

Where v_{ij} is the new position of employee bee, y_{ij} is the current position of employed bee, k is an arbitrary number between (1, N (population size)/2) $\neq$ i and j =1, 2,..., Number of design variables. R_{ij} is an arbitrary number between (-1, 1).
An onlooker bees chose a food source depending on the probability value related with that food source p_i , and is calculated using Equation (12).

$$P_i = \frac{F_i}{\sum_{n=1}^{N/2} F_n} \tag{12}$$

Where F_i is the fitness value of the solution i and N/2 is the number of food sources which is equal to the number of employed bees.

Onlooker bees get the information on class of the solutions from the employed bees, and select the solution with improved result. In Equation (12), a p_i probability is determined for each solution, the superior the quality of a solution, the higher its chance of being selected. Then, the onlooker bees search for fresh food source using (11) around the food source they have selected, and if the food source they find is superior, then they swap the old food source with the freshly found one.The Employed bee whose location of the food source cannot be enhanced for some predetermined number of cycles than that food source is called abandoned food source. That employed bee becomes scout and searches for the new solution arbitrarily using Equation (13).

$$y_i^j = y_{min}^j + rand(0,1)(y_{max}^j - y_{min}^j) \tag{13}$$

4. LEVY FLIGHTS

Levy flight [23] is a rank of non-Gaussian random processes whose arbitrary walks are drawn from Levy stable distribution. This allocation is a simple power-law formula $L(s) \sim |s|^{-1-\beta}$ where $0 < \beta < 2$ is an index. Mathematically exclamation, an easy version of Levy distribution can be defined as [24,25]:

$$L(s,\gamma,\mu) = \begin{cases} \sqrt{\frac{\gamma}{2\pi}} & exp\left[-\frac{\gamma}{2(s-\mu)}\right]\frac{1}{(s-\mu)^{3/2}} \quad if\ 0 < \mu < s < \infty \\ 0 \quad if\ s \leq 0 \end{cases} \tag{14}$$

where $\gamma > 0$ parameter is scale (controls the scale of distribution) parameter, μ parameter is location or shift parameter. In general, Levy distribution should be defined in terms of Fourier transform

$$F(k) = exp\left[-\alpha|k|^{\beta}\right], 0 < \beta \leq 2, \tag{15}$$

where α is a parameter within [-1,1] interval and known as scale factor. An index of 0 stability $\beta \in [0, 2]$ is also referred to as Levy index. The smaller β parameter causes the distribution to make longer jumps since there will be longer tail [26-28]. It makes longer jumps for smaller values whereas it makes shorter jumps for bigger values.

5. PROPOSED ENHANCED ARTIFICIAL BEE COLONY ALGORITHM

The ABC algorithm gives efficient results for most of the optimization problems. Although it is superior in setting the balance between exploration and exploitation compared to other algorithms, it has several deficiencies. While it can execute better the global search by acting arbitrary searches around each food source and cover the search space. Optimally, it meets several problems in the exploitation part, and gets stuck on local minimums particularly in complex multimodal

functions. If the original ABC algorithm flops to make enhancement for a particular food source as much as a predetermined limit value number, then the employed bee having that source become scout bee. Then this scout bee is arbitrarily distributed within the exploration space, boundaries of which are determined. In this case, scout bees select a zone within the exploration space completely in arbitrary mode without using the results found until that moment as a result of the iterations. It is a very low probability for this freshly selected food source to be better than the Global Min found until that moment. In this paper, in order to employ the scout bees better, they are made find a fresh food source using Levy Flight distribution with also the consequence of Global Min instead of selecting an arbitrary food source. By this way, it is sought to attain a better solution using the best food source until that moment instead of the food source that could not be improved. By executing enough arbitrary searches, exploration of the ABC algorithm, which is already noble in exploration, is enhanced. Let us assess in more detail how dispersal is performed using Levy flight. By Levy flight, new-fangled state of the particle is designed as

$$Y^{t+1} = Y^t + \alpha \oplus Levy\ (\beta) \tag{16}$$

α is the step size which must be related to the scales of the problem of interest. In the proposed EABCA method α is an arbitrary number for all dimensions of particles.

$$Y^{t+1} = Y^t + rand\left(size(Z)\right) \oplus Levy(\beta) \tag{17}$$

The product $\oplus$means entry-wise multiplications.
A non-trivial scheme of generating step size "A" samples are briefed as follows,

$$A = rand\left(size(Z)\right) \oplus Levy(\beta) \sim 0.01 \frac{u}{|v|^{1/\beta}}\left(y_j^t - gb\right) \tag{18}$$

where *u* and *v* are drawn from normal distributions. That is

$$u \sim R\left(0, \sigma_u^2\right) \quad v \sim R\left(0, \sigma_v^2\right) \tag{19}$$

With

$$\sigma_u = \left\{\frac{\Gamma(1+\beta)sin(\pi\beta/2)}{\Gamma[(1+\beta)/2]\beta 2^{(\beta-1)/2}}\right\}^{1/\beta}, \sigma_v = 1 \tag{20}$$

Here $\Gamma$is standard Gamma function. One of the important points to be considered while performing distribution by Levy flights is the value taken by the β parameter and it significantly affects distribution.

6. SIMULATION RESULTS

At first EABCA algorithm has been verified in IEEE 30-bus, 41 branch system. It has 6 generator-bus voltage magnitudes, 4 transformer-tap settings, and 2 bus shunt reactive compensators. Bus 1 is slack bus and 2, 5, 8, 11 and 13 are taken as PV generator buses and the rest are PQ load buses. Control variables limits are listed in Table 1.

Table 1: Preliminary Variable Limits (PU)

Variables	Min. Value	Max. Value	Type
Generator Bus	0.92	1.12	Continuous
Load Bus	0.94	1.04	Continuous
Transformer-Tap	0.94	1.04	Discrete
Shunt Reactive Compensator	-0.11	0.30	Discrete

The power limits generators buses are represented in Table 2. Generators buses (PV) 2,5,8,11,13 and slack bus is 1.

Table 2: Generators Power Limits

Bus	Pg	Pgmin	Pgmax	Qgmin
1	98.00	51	202	-21
2	81.00	22	81	-21
5	53.00	16	53	-16
8	21.00	11	34	-16
11	21.00	11	29	-11
13	21.00	13	41	-16

Table 3: Values of Control Variables after Optimization

Control Variables	EABCA
V1	1.0659
V2	1.0561
V5	1.0329
V8	1.0458
V11	1.0864
V13	1.0662
T4,12	0.00
T6,9	0.03
T6,10	0.91
T28,27	0.92
Q10	0.12
Q24	0.12
Real power loss	4.3052
Voltage deviation	0.9075

Table 3 shows the proposed approach succeeds in keeping the control variables within limits.
Table 4 summarizes the results of the optimal solution obtained by various methods.

Table 4: Comparison Results

Methods	Real power loss (MW)
SGA (29)	4.98
PSO (30)	4.9262
LP (31)	5.988
EP (31)	4.963
CGA (31)	4.980
AGA (31)	4.926
CLPSO (31)	4.7208
HSA (32)	4.7624
BB-BC (33)	4.690
EABCA	4.3052

Secondly the proposed hybrid EABCA algorithm is tested in standard IEEE-57 bus power system. The reactive power compensation buses are 18, 25 and 53. Bus 2, 3, 6, 8, 9 and 12 are PV buses and bus 1 is selected as slack-bus. The system variable limits are given in Table 5.

The preliminary conditions for the IEEE-57 bus power system are given as follows:
P_{load} = 12.422 p.u. Q_{load} = 3.339 p.u.
The total initial generations and power losses are obtained as follows:

$\sum P_G$ = 12.7729 p.u. $\sum Q_G$ = 3.4559 p.u.

P_{loss} = 0.27450 p.u. Q_{loss} = -1.2249 p.u.

Table 6 shows the various system control variables i.e. generator bus voltages, shunt capacitances and transformer tap settings obtained after EABCA based optimization which are within the acceptable limits. In Table 7, shows the comparison of optimum results obtained from proposed EABCA with other optimization techniques. These results indicate

the robustness of proposed EABCA approach for providing better optimal solution in case of IEEE-57 bus system.

Table 5: Variable limits

Reactive Power Generation Limits							
Bus no	1	2	3	6	8	9	12
Qgmin	-1.4	-.015	-.02	-0.04	-1.3	-0.03	-0.4
Qgmax	1	0.3	0.4	0.21	1	0.04	1.50

Voltage And Tap Setting Limits					
vgmin	vgmax	vpqmin	vpqmax	tkmin	tkmax
0.5	1.0	0.91	1.01	0.5	1.0

Shunt Capacitor Limits			
Bus no	18	25	53
Qcmin	0	0	0
Qcmax	10	5.2	6.1

Table 6: control variables obtained after optimization

Control Variables	EABCA
V1	1.2
V2	1.070
V3	1.061
V6	1.049
V8	1.068
V9	1.039
V12	1.049
Qc18	0.0850
Qc25	0.341
Qc53	0.0631
T4-18	1.020
T21-20	1.060
T24-25	0.961
T24-26	0.939
T7-29	1.079
T34-32	0.940
T11-41	1.010
T15-45	1.061
T14-46	0.930
T10-51	1.040
T13-49	1.061
T11-43	0.910
T40-56	0.904
T39-57	0.961
T9-55	0.971

Table 7: comparison results

S.No.	Optimization Algorithm	Finest Solution	Poorest Solution	Normal Solution
1	NLP [34]	0.25902	0.30854	0.27858
2	CGA [34]	0.25244	0.27507	0.26293
3	AGA [34]	0.24564	0.26671	0.25127
4	PSO-w [34]	0.24270	0.26152	0.24725
5	PSO-cf [34]	0.24280	0.26032	0.24698
6	CLPSO [34]	0.24515	0.24780	0.24673
7	SPSO-07 [34]	0.24430	0.25457	0.24752
8	L-DE [34]	0.27812	0.41909	0.33177
9	L-SACP-DE [34]	0.27915	0.36978	0.31032
10	L-SaDE [34]	0.24267	0.24391	0.24311
11	SOA [34]	0.24265	0.24280	0.24270
12	LM [35]	0.2484	0.2922	0.2641
13	MBEP1 [35]	0.2474	0.2848	0.2643
14	MBEP2 [35]	0.2482	0.283	0.2592
15	BES100 [35]	0.2438	0.263	0.2541
16	BES200 [35]	0.3417	0.2486	0.2443
17	Proposed EABCA	0.22349	0.23472	0.23129

Then EABCA has been tested in standard IEEE 118-bus test system [36] .The system has 54 generator buses, 64 load buses, 186 branches and 9 of them are with the tap setting transformers. The limits of voltage on generator buses are 0.95, -1.1 per-unit., and on load buses are 0.95, -1.05 per-unit. The limit of transformer rate is 0.9, -1.1, with the changes step of 0.025. The limitations of reactive power source are listed in Table 8, with the change in step of 0.01.

Table 8: Limitation of reactive power sources

BUS	5	34	37	44	45	46	48
QCMAX	0	14	0	10	10	10	15
QCMIN	-40	0	-25	0	0	0	0
BUS	74	79	82	83	105	107	110
QCMAX	12	20	20	10	20	6	6
QCMIN	0	0	0	0	0	0	0

In this case, the number of population is increased to 120 to explore the larger solution space. The total number of generation times is set to 200. The statistical comparison results of 50 trial runs have been list in Table 9 and the results clearly show the better performance of proposed algorithm.

Table 9: Comparison results

Active power loss (p.u)	BBO [37]	ILSBBO/ strategy1 [37]	ILSBBO/ strategy1 [37]	Proposed EABCA
min	128.77	126.98	124.78	120.98
max	132.64	137.34	132.39	129.99
Average	130.21	130.37	129.22	123.81

7. CONCLUSION

Enhanced Artificial Bee Colony Algorithm has been effectively applied for Optimal Reactive Power dispatch problem. Enhanced Artificial Bee Colony Algorithm based optimal reactive power problem has been tested in standard IEEE30, 57,118 bus systems. Performance comparisons with standard population-based algorithms have given encouraging results. Real power loss has been considerably reduced and control variables are well within the limits. Enhanced Artificial Bee Colony Algorithm emerges successfully to find good solutions when compared to that of other algorithms. The simulation results presented in previous section prove the ability of Enhanced Artificial Bee Colony Algorithm approach to arrive at near global optimal solution.

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NODE SCALABILITY OF ICDAiLEACH: INTER CLUSTER DATA AGGREGATION BASED iLEACH

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ABSTRACT

Energy consumption have found to be crucial issue in WSNs. Data aggregation techniques have become a major part of WSNs to overcome the problem energy consumption by reducing the flooding at the base station. Moreover, data aggregation techniques reduce the communication cost of WSNs because it reduces the redundant data by aggregation. However, certain improvements have been proposed for the cluster head selection optimization as well to enhance the lifetime further. The overall objective of this paper is to evaluate the performance of the LEACH, iLEACH, DA_LEACH and PROPOSED_DA by considering different number of nodes i.e. 100, 200 & 300. The experimental results show that PROPOSED_DA outperforms above the available techniques with reverence to stability period and network lifetime.

Keywords—*LEACH, iLEACH, DA_LEACH, Wireless sensor networks, Network lifetime*

1. INTRODUCTION

A wireless sensor network (WSN) is defined as a network of probably low-size, low-battery power and low-complex devices denote as nodes that can sense the environment and communicate the information gathered from the monitored field throughout wireless links; the sense data is forward, possibly by multiple hops relay to a sink or controller that can utilize it locally or is connected to other networks (e.g. the Internet) through a gateway.

A node in sensor network consists of CPU used for data processing, memory used for data storage, battery used for energy and transceiver used for receiving and sending signals. The size of every sensor node varies with application. The nodes can be stationary or moving. They can be location-aware or not. They can be homogeneous or heterogeneous. Each node has the capability to sense elements of its environment, achieve simple computations, and communicate along with its peers or directly to an external Base Station (BS). A base station might be a fixed node or a mobile node capable of connecting the sensor network to an existing communications infrastructure or to the Internet where a user can have access to the reported data. The key applications of WSNs are habitat monitoring, target tracking, surveillance, and security management. Figure 1 shows the architecture of WSN.

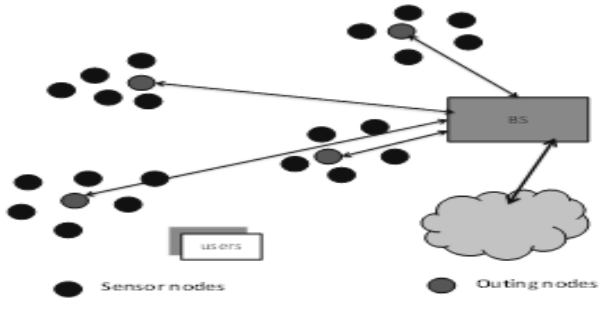

Figure.1 A wireless sensor network structure

There are many challenges in WSN and the key challenge is to maximize the stability as well as lifetime of network. It is not possible to replace the batteries of hundreds or thousands of sensor nodes after deployment. In WSN, grouping of sensor nodes into a cluster is called clustering. Clustering is generally adopted in WSNs in which the whole network is divided into multiple clusters. Clusters have cluster heads (CHs) responsible for data aggregation. It has the advantages of low energy consumption, simple routing scheme as well as good quality scalability. Mainly traditional clustering routing protocols for WSNs are based on homogeneous networks wherever all sensor nodes are identical in terms of battery energy and hardware configuration.

2. DATA AGGREGATION

In typical WSNs, sensor nodes are usually resource-constrained and battery-limited. In order to save resources and energy, data must be aggregated to avoid overpowering amounts of traffic in the network. There has been extensive work on data aggregation schemes in sensor networks. The aim of data aggregation is that eliminates redundant data transmission and enhances the lifetime of energy in WSNs. Data aggregation (DA) is the process of one or several sensors then collects the detection result from other sensor. The collected data must be processed by sensor to decrease transmission burden before they are transmit to the BS or sink. The WSN consist of three types of nodes: Simple regular sensor nodes, aggregator node and querier. Regular sensor nodes sense data packet from the environment and send to the aggregator nodes. These aggregator nodes collects data from multiple sensor nodes of the network, aggregates the data packet using some aggregation functions like sum, average, count, max, min and then sends aggregates result to upper aggregator node or the querier node who generates the query.

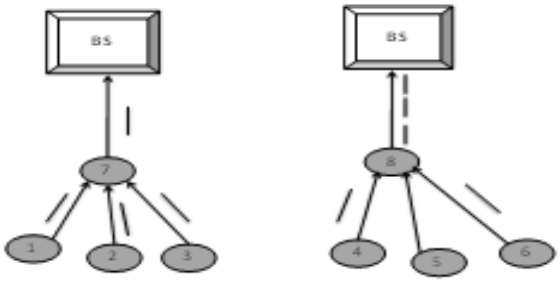

Figure.2 Data aggregation model and Non-data aggregation model

It can be the BS or sometimes an external user who has permission to interact with the network. Data transmission between sensor nodes, aggregators and the querier consumes a lot of energy in WSNs. Figure 2 contain two models, one is data aggregation model and the second is non-data aggregation model in which sensor nodes 1, 2, 3,4,5,6 are regular nodes that collects data packet and report them back to the upper nodes where sensor nodes 7, 8 are aggregators that perform sensing and aggregating at the same time. In this aggregation model, 4 data packet travelled within the network and only one data packet is transmitted to the BS and other non-data aggregation model also 4 data packet travelled within the network and all data packets are sent to the BS. With the help of data aggregation process, decrease the number of data packet transmission and also save energy of the sensor node in the WSN. With the help of data aggregation, we improve the lifetime of WSN. Sink have a data packet with energy-efficient way with minimum data latency. So, data latency is very important in numerous applications of WSNS such as environment monitoring, health, monitoring, wherever the freshness of data is also a significant feature. It is vital to develop energy-efficient data-aggregation algorithms so that network lifetime is enhanced. There are various data aggregation techniques in WSN:

1.1 CLUSTER-BASED APPROACH In energy-constrained sensor networks of large size, it is inefficient for sensors to transmit the data directly to the BS. Cluster based approach is a hierarchical approach. In cluster-based approach, whole network is divided into several clusters. Each cluster has a cluster-head which is selected among cluster members.

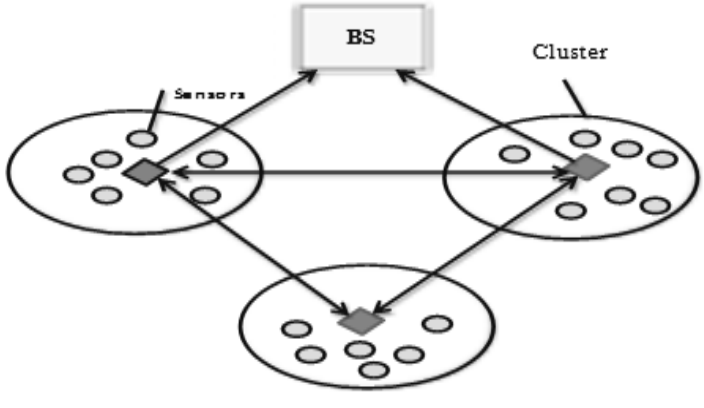

Figure.3 Cluster based sensor network. The arrows indicate wireless communication links.

Cluster-heads do the role of aggregator which aggregates data received from cluster members locally and then transmit the result to BS. Several cluster-based network organization and data-aggregation protocols have been proposed for the WSN. Figure 3 shows a cluster-based sensor network organization. The cluster heads can communicate with the sink directly via long range transmissions or multi hopping through other cluster heads.

1.2 TREE-BASED APPROACH The tree-based approach is defining aggregation from constructing an aggregation tree. The form of tree is minimum spanning tree, sink node consider as a root and source node consider as leaves. Information flowing of data starts from leaves node up to root means BS. Disadvantage of this approach, like WSNs are not free from

failure, in case of data packet loss at any level of tree, the data will be lost not only for single level but for whole related sub tree as well. This approach is suitable for designing optimal aggregation techniques.

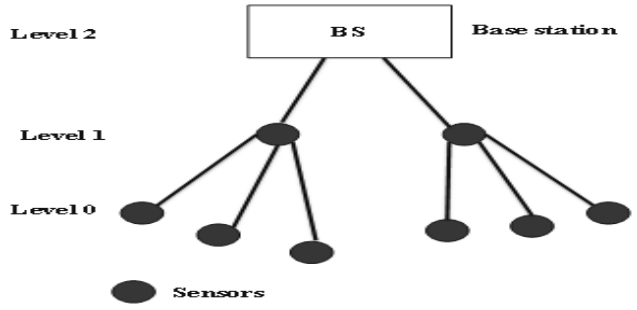

Figure.4 Tree-based data aggregation

1.3 HYBRID-BASED APPROACH Hybrid-based approach follow between tree and cluster based scheme. In this, the data aggregation structure can be adjusted according to particular network situation and to various performance statistics.

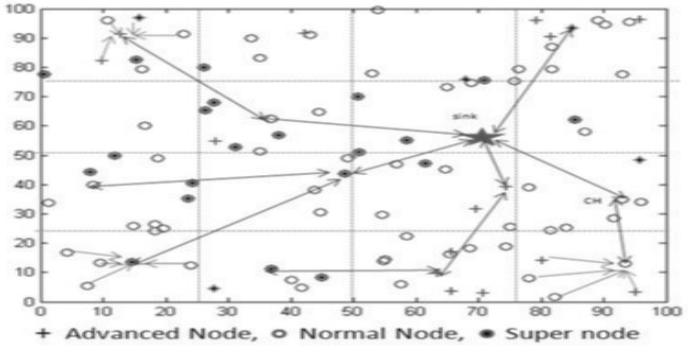

Figure.5 Hybrid based approach (1)

There are three types of sensor nodes: normal, advance and super. To become cluster head in a round, normal nodes utilize residual energy base scheme. Advance and super nodes act as relay node to reduce the transmission load of a normal node cluster head when they are not cluster heads in a round. The super nodes have two transceivers: one connects to the WSN, and the other connects to the super node network. The super node network provide enhanced QoS and is used to rapidly forward sensor data packets to the user. Super nodes could process sensor data before forward. The hybrid based approach shown in figure 5 distributes nodes at random with different energy levels as normal node, advanced node and super node through mobile sink.

Let C_i denote the cluster formed by CH node 'i' with neighbor nodes N_i, and then cost of aggregation with cluster C_i is define as:

$$C_i = \sum_{j \in N_i} cost(j,i) + cost(i, \sin k)$$

This indicate the cost of data aggregation in terms of energy consumption by the network, where cluster members send random packets to CH [cost (j, i)] and CH to sink [cost (i, sink)]. To aggregate the data packets the aggregation functions at CH is defined as:

$$f(C_A) = \sum_{i=1}^{K} (X_i) + \frac{1}{M} \sum_{j=1}^{M} (Y_j)$$

Where X_i and Y_i are variables that represent the correlation of the number of data packets generated by participating nodes in the cluster.

3. RELATED WORK

BHCDA use the absolutely compressible aggregation function [1] to enhance the bandwidth utilization and energy saving as compare with EECDA. The aggregation ratio [2] increases as the number of nodes and their density in the network increase compare to other solutions that are not affected by the parameters. An energy efficient routing algorithm has been proposed which save an important section of inner-network [3] communications energy. Reduced energy consumption in transmission [4] of aggregated data indicates profit of the increase in a lifetime of the network. EERDAT use that energy has been reduced effectively and reliability has been maintained as the size of the cluster is altered based upon the loss ratio [5]. MAC protocol has been use for an emergency event which takes the benefit of both contention [6] and TDMA alongside with the data aggregation approach. It can be experimental that there has a significant enhancement in the network lifetime in ILEACH protocol comparison [7] to the LEACH protocol. The remainder power [8] of the sensor nodes in order to balance network loads as well as change the round time depends on the optimal cluster size. A multi-metrics protocol takes the trade-off [9] between data quality and energy consumption use to increase the lifetime of WSN. A

novel technique of choose cluster-heads has been used which decrease redundant consumption of energy [10] spend on compute of each node through each round. E2IPAP considerably reduces the overhead [11] in disseminate off-path values and overall communication. E2IPAP has secure data aggregation protocols. SHM prototype demonstrates the advantages of performing flexible data aggregation for energy-efficient and intelligent monitoring. Cluster-based data aggregation mechanism can save energy and optimize [12] the sharing of computing tasks. DAWN use a number of motion strategy [13] for mobile sinks to reduce the energy consumption beneath different data collection necessities. DCDA-LEACH has the advantages of energy efficiency [14] and even distribution of energy consumption. The actual effect of DCDA-LEACH to expand the network life cycle depends on the importance of the measured data in the specific application. PDA can protect the trend of private data [15] of a sensor node from being known by its neighboring nodes and data aggregators in a WSN. DAMS (Distributed data Aggregation active Monitoring System) above all designed for the wireless sensor network used in bridge diagnosis [16]. The DAMS can accurately monitor the nodes health status and link quality in the wireless sensor network. Data redundancy is essential for secured transmission [17] and privacy in interference limited and noisy environment. A highly secured data aggregation method has been used which ensures that information of all live nodes inside the network is accessible inside the sink node with the minimum redundancy. In this, data of all live nodes stored in the sink are accessible inside the sink even if the wireless channel is polluted with noise and interference.

4. LEACH

LEACH stands for Low-Energy Adaptive Clustering Hierarchy. It is the first hierarchical routing protocol in Wireless Sensor network. In this protocol nodes are divided into only two types of categories; normal sensor nodes and cluster heads (CH). At first the normal sensor nodes are grouped together and form clusters and among all the sensor nodes in a cluster one node are selected as a CH node. Figure 6 depict a WSN protocol based on LEACH which is divided into three clusters, the black circle in each cluster represent the cluster head, and the white circles show non-cluster head nodes. Each cluster has a cluster head node. The protocol randomly selects cluster head node circularly, the energy of the whole network load is equally distributed to each sensor node which can attain lower energy consumption and improve the network lifetime.

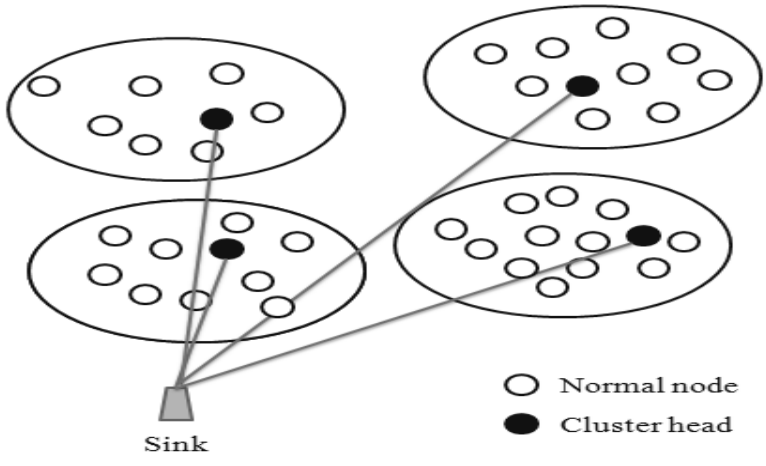

Figure.6 Architecture of LEACH

The CH selection method is a random selection method where every node is assign a random value and this is compare with a threshold value T_n. If the nodes random value is less than the T_n, then the particular node can act as a CH. The threshold for the node T_n is given as:

$$T_n = \begin{cases} \dfrac{P}{1 - P \times \left(r \bmod \frac{1}{P}\right)}, & n \in G \\ 0, & Otherwise \end{cases}$$

Where n is the given number of nodes, p is the probability of a node being elected as a cluster-head, r is a random number between 0 and 1 that is selected by a sensor node, mod denotes modulo operator, G is the set of nodes that were not accepted as cluster head in the last "1/p" events. At first normal sensor nodes transmit their data to their respective CHs. On receiving these data, the CHs aggregated them in a compressed form and further transmit them to the BS. Finally BS received all compressed data from different CHs present in the network. Although LEACH protocol acts in a good manner, it also suffers from many drawbacks such as:

- CHs selection is random, which does not take into account the residual energy of every node.
- The high frequency of selecting CHs wastes a certain amount of energy.
- It can't cover a large area. CHs are not uniformly distributed, where CHs can be located at the edge of the cluster.

5. iLEACH

The improved LEACH (iLEACH) protocol is based on the initial energy and number of neighbors of the nodes. This protocol is more applicable than any type that assumes a protocol in which each node knows the total energy of the network and then adapts its election probability of becoming a cluster head according to its remaining energy.

$$T_{n=}\begin{cases}\dfrac{p}{1-p\left(r \bmod\left(\frac{1}{p}\right)\right)} \times \dfrac{E_{cur}}{E_{avg}} \times \dfrac{Nbr_n}{Nbr_{avg}} \times \dfrac{dtobs_{avg}}{dtobs_n} S \in G\end{cases}$$

Where E_{cur} is the current sensor node power E_{avg}; is the average energy of the network in the current round; Nbr_n is the number of neighbors for *n*; Nbr_{avg} is the average number of neighboring nodes in the network; $dtobs_{avg}$ is the average distance of the network sensor nodes to the BS; $dtobs_n$ is the distance of sensor nodes from the BS. The more is the distance of the sensor node far from the BS, the more is the amount of energy spent on sending data to the BS.

6. RESEARCH GAPS AND MOTIVATIONS

To evaluate the gaps in existing research; latest published papers of some well-known journals have been evaluated.

1. The survey has shown that the most of the existing data aggregation techniques are for limited battery WSNs. But in real time applications WSNs comes up with heterogeneous sensor nodes.
2. Many WSNs data aggregation at the base station by individual nodes causes flooding of the data which consequences in maximum energy consumption.
3. Also most of data aggregation methods are either based upon the clustering or tree-based approach but the use of hybrid data aggregation has been ignored by the most of the researchers.

7. ALGORITHM

INTER-CLUSTER DATA AGGREGATION BASED iLEACH

/*Initialization of WSN*/

1. *Firstly nodes are deploy at random.*
2. *Identification of normal nodes:*

   $if(tamplifier\_\max\_do\_rndo \geq (m+x) \times n + 1)$

3. $S(i).E = E_o$ // E_o = Initial energy
4. *endif*

/*Setup phase*/

$T_{n=}\begin{cases}\dfrac{p}{1-p\left(rmod\left(\frac{1}{p}\right)\right)} \times \dfrac{E_{cur}}{E_{avg}} \times \dfrac{Nbr_n}{Nbr_{avg}} \times \dfrac{dtobs_{avg}}{dtobs_n} S \in G\end{cases}$ // n is the given number of nodes, p is the probability of a node being elected as a cluster-head, r is a random number between 0 and 1 that is selected by a sensor node, mod denotes modulo operator,

// G is the set of nodes that were not accepted as cluster head in the last 1/p events, E_{cur} is current sensor node power, E_{avg} is the average energy of the network in the current round, Nbr_n is the number of neighbors for *n*, Nbr_{avg} is the average number of neighboring nodes in the network, $dtobs_{avg}$ is the average distance of the network sensor nodes to the BS, $dtobs_n$ is the distance of sensor nodes from the BS.

5. *Elect CH show the message to sensor nodes(SNs).*
6. *CH assign TDMA schedule to cluster members(CMs)*/*Transmission phase1*/
7. *for CH, for CMs*
8. *Data sent from CMs to CH as per TDMA schedule.*
9. *Intracluster Data aggregation via accessible data aggregation functions:*

(a) $Addition = \sum_{i=1}^{X}(A_i)$ for $\forall(A_i)$ = *Discrete Data* // i=1…X, X= nodes having different data packets.

(b) $Division = \frac{1}{Y}\sum_{j=1}^{Y}(B_j)$ for $\forall(B_j) = Comparable\ data$

// j=1…Y, Y= nodes having similar data packets.

10. *end for CMs*

/* Relay node selection*/

11. *for relay node*
12. *while status* $= 0$ // node is not processed
13. *find distance between current_CH and BS using Euclidean distance:*
    $distance = \sqrt{(x_1 - x_2)^2 + (y_1 - y_2)^2}$
14. *if distance* < min_distance *then*
15. *Allocate distance to* min *_distance*
16. *Allocate current_CH to relay node*
17. *end if*
18. *end while*
19. *Set status* $= 1$ // node is processed

/*Transmission phase2*/

20. *Send data from CHs to relay node.*
21. *End for CH*
22. *Intercluster DA using Additive DA*

i. $\forall j \in CH$ // for each node belong to cluster head

ii. $if\ j.status = 'Inactive'$ // check the status whether it is active or inactive in which active means it has been added for data aggregation previously and inactive means it require data aggregation

iii. $if(\max\ \_data) = \emptyset$ Then // $(\max\ \_data)$ is a type of frame which hold the aggregated data.

iv. $Assign\ j.data$ to $\max\ \_data$

v. $Set\ j.status = 'Active'$ // not necessary to aggregate data of j again and again.

vi. *else if* $\max\ \_data + j.data \leq channel\_limit$ Then // $channel\_limit$ is the maximum capability of transfer data of WSN.

vii. $Assign\ \max\ \_data + j.data$ to $\max\ \_data$

viii. $Set\ j.status = 'Active'$

xi. *else* $\max\ \_data + j.data \leq channel\_limit$ Then

x. $Assign\ \max\ \_data$ To $additive\_packet(m$ // $additive\_packet(m)$ is a complete label.

xi. $Put(\max\ \_data) = \emptyset$

xii. $m = m + 1$ // Initialize a new additive packet

xiii. *Repeat steps (iii) to (xii) till the statu of all CHs not equal to inactive.*

xiv. *end, end*

/*Transmission phase3*/

23. *Send compressed data from relay node to BS.*
24. *End for relay node*
25. *Apply divisible data aggregation at BS*

i. *Repeat step 5.*

ii. *While the count_additive_packet not equal to ZERO*

iii. *Extract data from packet (count_additive_packet) and Set count_additive_packet = count_additive_paket − 1.*

iv. *Finish*

26 *End of code*

8. EXPERIMENTAL SETUP

The performance of different homogeneous protocols has been evaluated in MATLAB. The simulation has been peformed in the network of 100 nodes and the base station. The nodes are placed randomly in the network and the field size is 100m x100m. The performance of LEACH, iLEACH, DA_LEACH and PROPOSED_DA has been compared. Here, use different metrics to analyze and compare the performance of the protocols which are first dead evaluation, all dead node evaluation, average remaining energy and number of alive nodes.

Table 1Value of Parameters

Parameter	Values
Area (x, y)	100,100
Base station (x, y)	50,150
Nodes (n)	100
Probability (p)	0.1
Initial Energy	0.1
transmitter energy	$50* 10^{-9}$
receiver energy	$50* 10^{-9}$
Free space(amplifier)	$10 * 10^{-13}$
Multipath(amplifier)	$0.0013* 10^{-13}$
Effective Data aggregation	$5* 10^{-9}$
Maximum lifetime	800

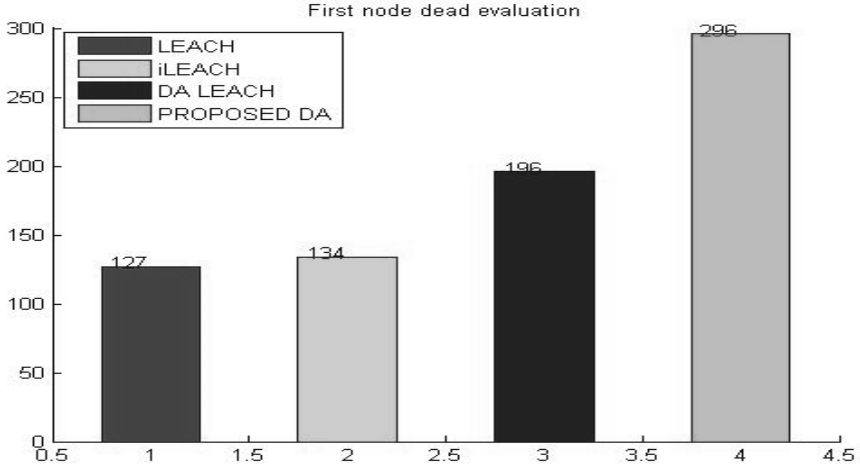

Figure.7 First node dead evaluation

Now, considering first case in which parameter changes to nodes is equal to 100. Figure 7 shows that the first dead node appears at round 127 in LEACH while the first dead node appears at round 134 in iLEACH while the first dead node appears at round 196 in DA_LEACH as well as the first dead node appears at round 296 in PROPOSED_DA. Therefore, the

performance of iLEACH is better than that of LEACH whereas DA_LEACH is better than iLEACH as well as PROPOSED_DA is better than DA_LEACH. So, the simulation shows that the performance of PROPOSED_DA is better than LEACH, iLEACH and DA_LEACH.

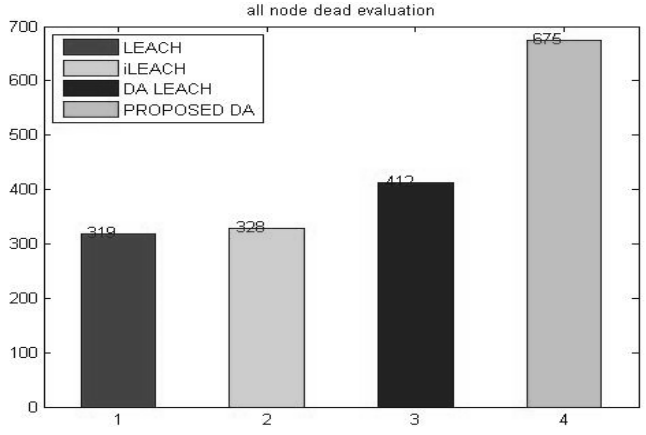

Figure.8 All node dead evaluation

Figure 8 shows that all dead node appears at round 319 in LEACH while the all dead node appears at round 328 in iLEACH while all dead node appears at round 413 in DA_LEACH as well as all dead node appears at round 676 in PROPOSED_DA. Therefore, the performance of iLEACH is better than that of LEACH whereas DA_LEACH is better than iLEACH as well as PROPOSED_DA is better than DA_LEACH. So, the simulation shows that the performance of PROPOSED_DA is better than LEACH, iLEACH and DA_LEACH.

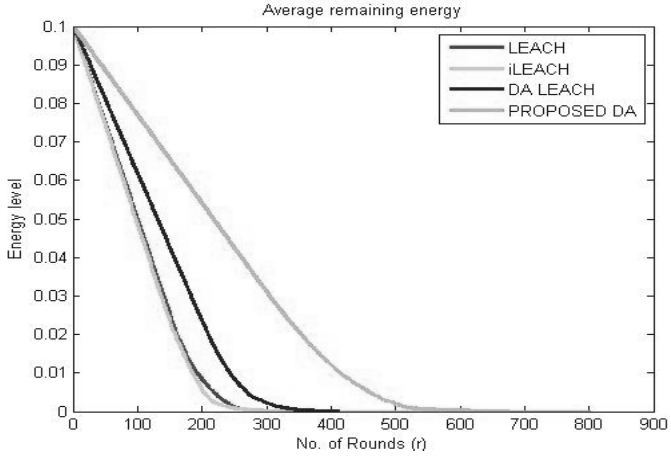

Figure.9 Average remaining energy during rounds

Figure 9 shows that the average remaining energy in the network is optimally managed. The average remaining energy in LEACH has been reduced compared with iLEACH, as well as remaining energy in DA_LEACH has been reduced than iLEACH. In this, average remaining energy in LEACH and iLEACH has been overlapped due to the trade-off factor. As well as the performance of DA_LEACH is better than both LEACH and iLEACH. The PROPOSED_DA shows the better results than all other.

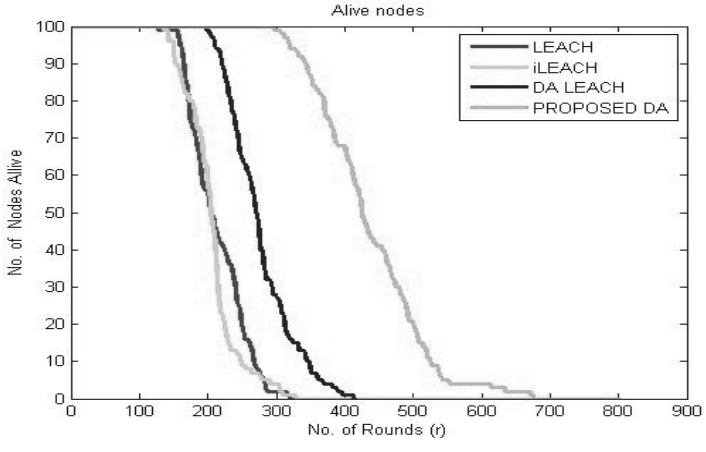

Figure.10 Alive nodes during rounds

Figure 10 shows network lifetime of all routing protocols. By comparing LEACH, iLEACH, DA_LEACH and PROPOSED_DA, the stability period of iLEACH is shorter than LEACH as well stability period of DA_LEACH is better than iLEACH. DA_LEACH performs better results than LEACH and iLEACH. The network lifetime of DA_LEACH is better than other. But the stability period of PROPOSED_DA is better among all of them.

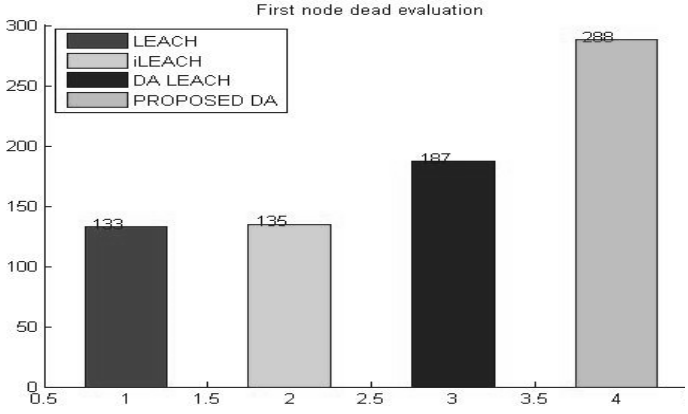

Figure.11 First node dead evaluation

Now, considering the second case in which parameter changes to nodes that is equal to 200. Figure 11 shows that the first dead node appears at round 133 in LEACH while the first dead node appears at round 135 in iLEACH while the first dead node appears at round 187 in DA_LEACH as well as the first dead node appears at round 288 in PROPOSED_DA. Therefore, the performance of iLEACH is better than that of LEACH whereas DA_LEACH is better than iLEACH as well as PROPOSED_DA is better than DA_LEACH. So, the simulation shows that the performance of PROPOSED_DA is better than LEACH, iLEACH and DA_LEACH.

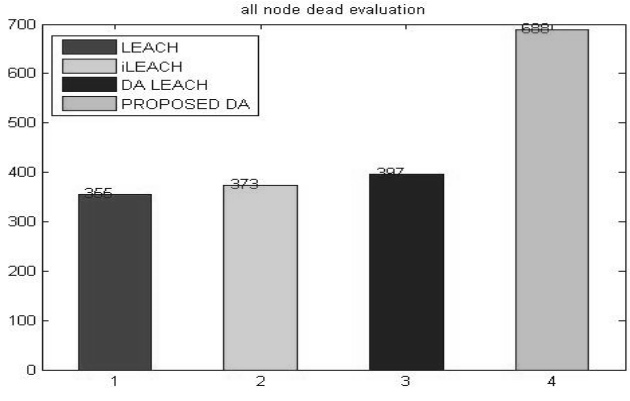

Figure.12 All node dead evaluation

Figure 12 shows that all dead node appears at round 355 in LEACH while the all dead node appears at round 373 in iLEACH while all dead node appears at round 397 in DA_LEACH as well as all dead node appears at round 688 in PROPOSED_DA. Therefore, the performance of iLEACH is better than that of LEACH whereas DA_LEACH is better than iLEACH as well as PROPOSED_DA is better than DA_LEACH. So, the simulation shows that the performance of PROPOSED_DA is better than LEACH, iLEACH and DA_LEACH.

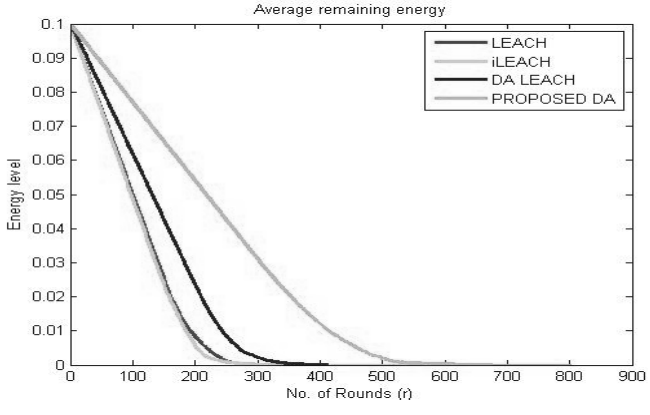

Figure.13 Average remaining energy during rounds

Figure 13 shows that the average remaining energy in the network is optimally managed. The average remaining energy in LEACH has been reduced compared with iLEACH, as well as remaining energy in DA_LEACH has been reduced than iLEACH. In this, average remaining energy in LEACH and iLEACH has been overlapped due to the trade-off factor. As well as the performance of DA_LEACH is better than both LEACH and iLEACH. The PROPOSED_DA shows the better results than all other.

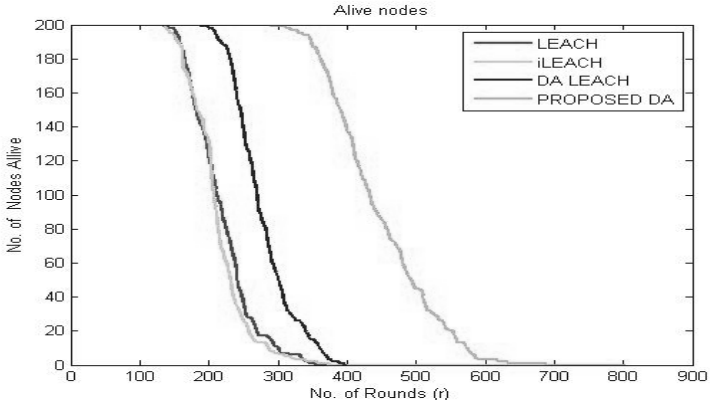

Figure.14 Alive nodes during rounds

Figure 14 shows network lifetime of all routing protocols. By comparing LEACH, iLEACH, DA_LEACH and PROPOSED_DA, the stability period of LEACH and iLEACH is almost same i.e. it overlaps due to trade-off factor. The stability period of DA_LEACH is better than LEACH and iLEACH. The network lifetime of DA_LEACH is better than other. But the stability period of PROPOSED_DA is better among all of them. So, network lifetime of PROPOSED_DA is better among all.

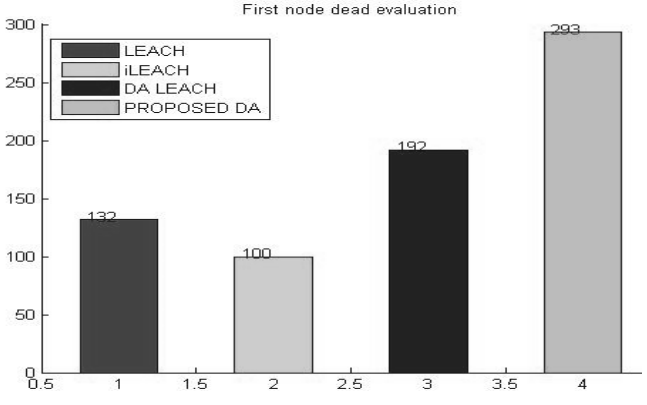

Figure.15 First node dead evaluation

Now, considering third case in which parameters changes to nodes is equal to 300. Figure 15 shows that the first dead node appears at round 132 in LEACH while the first dead node appears at round 100 in iLEACH while the first dead node appears at round 192 in DA_LEACH as well as the first dead node appears at round 293 in PROPOSED_DA. Therefore, the performance of LEACH is better than that of iLEACH whereas DA_LEACH is better than iLEACH as well as PROPOSED_DA is better than DA_LEACH. So, the simulation shows that the performance of PROPOSED_DA is better than LEACH, iLEACH and DA_LEACH.

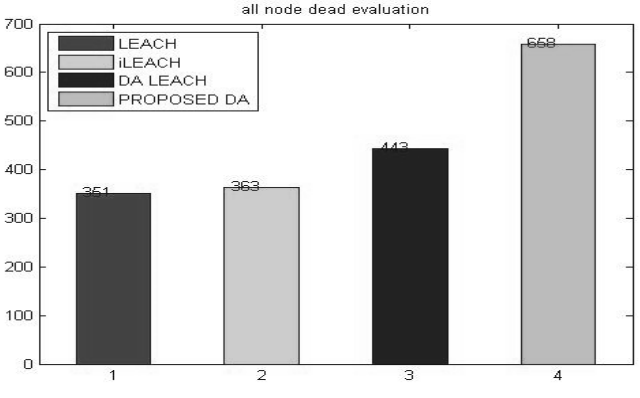

Figure.16 All node dead evaluation

Figure 16 shows that all dead node appears at round 361 in LEACH while the all dead node appears at round 363 in iLEACH while all dead node appears at round 443 in DA_LEACH as well as all dead node appears at round 658 in

PROPOSED_DA. Therefore, the performance of iLEACH is better than that of LEACH whereas DA_LEACH is better than iLEACH as well as PROPOSED_DA is better than DA_LEACH. So, the simulation shows that the performance of PROPOSED_DA is better than LEACH, iLEACH and DA_LEACH.

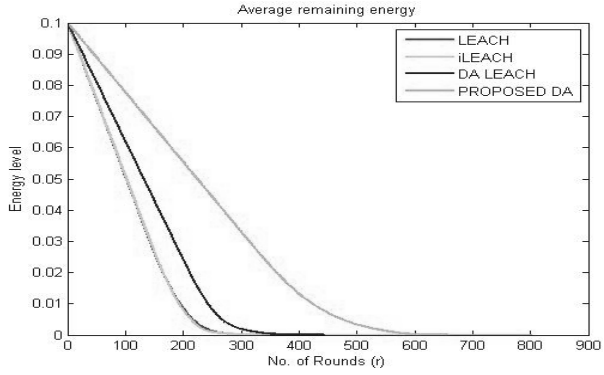

Figure.17 Average remaining energy during rounds

Figure 17 shows that the average remaining energy in the network is optimally managed. The average remaining energy in LEACH has been reduced compared with iLEACH, as well as remaining energy in DA_LEACH has been reduced than iLEACH. In this, average remaining energy in LEACH and iLEACH has been overlapped due to the trade-off factor. As well as the performance of DA_LEACH is better than both LEACH and iLEACH. The PROPOSED_DA shows the better results than all other.

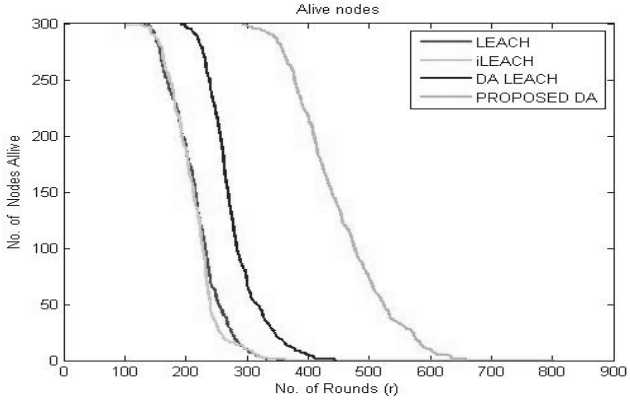

Figure.18 Alive nodes during rounds

Figure 18 shows network lifetime of all routing protocols. By comparing LEACH, iLEACH, DA_LEACH and PROPOSED_DA, the stability period of LEACH and iLEACH have almost same i.e. it overlaps due to which trade-off factor exists. The stability period of DA_LEACH is better than LEACH and iLEACH. The network lifetime of DA_LEACH is better than other. But the stability period of PROPOSED_DA is better among all of them. So, network lifetime of PROPOSED_DA has been better among all.

Table 2, 3and 4 shows the value of first and all node dead evaluation when number of nodes is deployed. The protocols are LEACH, iLEACH, DA_LEACH and PROPOSED_DA.

Table 2 Comparative analysis when n=100

Protocols	First node dead	All node dead
LEACH	127	319
iLEACH	134	328
DA_LEACH	196	412
PROPOSED_DA	296	676

Table 3 Comparative analysis when n=200

Protocols	First node dead	All node dead
LEACH	133	355
iLEACH	135	373
DA_LEACH	187	397
PROPOSED_DA	288	688

Table 4 Comparative analysis when n=300

Protocols	First node dead	All node dead
LEACH	132	361
iLEACH	100	363
DA_LEACH	192	443
PROPOSED_DA	293	658

Table 2, 3 and 4 has shown that iLEACH performs better than the LEACH whereas DA_LEACH performs better than iLEACH whereas PROPOSED_DA performs better than DA_LEACH. Hence, PROPOSED_DA outperforms among LEACH, iLEACH, DA_LEACH and PROPOSED_DA even in the case of scalability of sensor nodes.

9. CONCLUSION AND FUTURE SCOPE

The energy and bandwidth of the sensors are valued resources along with important to consume proficiently. Data aggregation at the base station by individual nodes causes flooding of the data which consequences in most energy consumption. To modest this problem, numerous data aggregation techniques have been proposed so far. It has been found that the majority of the clustering based protocol has focused on inter-cluster data aggregation. This paper has evaluated the performance of the LEACH, iLEACH, DA_LEACH and PROPOSED_DA by using the MATLAB tool.

It has been found the PROPOSED_DA outperforms over the LEACH, iLEACH and DA_LEACH together either stability period or network lifetime under different set of sensor nodes (100,200,300). But between LEACH and iLEACH there exists trade-off in terms of stability period and the network lifetime. If stability period or network lifetime considered then iLEACH is better than the LEACH. Therefore, the PROPOSED_DA is quite better and found to be best choice among LEACH, iLEACH and DA_LEACH and PROPOSED_DA.

In near future, a new hybrid data aggregation based clustering protocol will be proposed to enhance the outcome of clustering protocol further. Moreover, the use of data compression technique at CHs will also be done to diminish the data packets size to utilize the network bandwidth accurately.

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FIXTURE DESIGN FOR GRID FRAME TO IMPROVE ROBOT WELDING PRODUCTIVITY AND PROFITABILITY

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ABSTRACT

Today in the world of modern market, customer demand for a variety with quick and effective responds for which manufacturers need to ensure that their manufacturing practices are sufficiently flexible to achieve rapid product development. Fixtures which secure workpieces during machining so that they can be changed into parts with required design qualifications, is a significant contributing factor towards achieving manufacturing flexibility. Thus, for achieving these, fixture can be developed in Computer Aided Fixture Design (CAFD). This paper contains the basic ideas of fixture design with clamping positions for the grid frame model. Various design of fixture is recommended to the industry for increase the production with good quality and less fatigue of an operator with the help of CAFD. The primary use of CAFD was to apply CAD software as a tool for designing and assembling fixture elements by employing a regular fixture collection. As fixtures are mostly used in manufacturing and have a great impact on upon product manufacturing excellence, efficiency and cost so much attention has been paid in the industries before developed it. Case Based Reasoning method is used as optimization method for getting the modified fixture with the available data of the current one. The methods for case retrieval, reuse, solution testing, and learning are summarized, and their actual realization is discussed that represent CBR approaches. By means of these steps the assembly time of the product on fixture has reduce which results in increase of productivity and profitability of industry.

Keywords – *Fixture design, CAFD, CBR*

1. INTRODUCTION

The fixture is a unique tool for holding a work piece in suitable position during its built-up operation. In other words a system used to situate a work piece, locate it properly with respect to a machine tool, and hold it during operation performed on it is a fixture. Fixtures are used to firmly situate (position in a specific location or direction) and hold the work, ensuring that all parts formed using the fixture will continue consistency and interchangeability. Use of fixture allows smooth action and speedy change from part to part, reducing the necessity for expert labour by simplifying how work pieces are mounted, and increasing conventionality across a production run which lastly improves the economy of the production. Fixtures are always be designed with economics in mind whose reason is to cut costs, and so they must be designed in such a way that the cost reduction which also overcome the cost of implementing the fixture. Thus, Fixture design is a difficult task which is carried out by considering its built-up behavior. With the use of Computers in the designing method the time for fixture designer has been reduced and is called as computer aided fixture design (CAFD). By using a computer,

designers are capable to design in a virtual situation. This will helps the designers to identify potential problems and undertake different ideas without truly creating the fixture. These programs have added the benefit of keeping a designer from missing steps while designing, and by avoiding mistakes time and costs can be kept low. Thus, Computer Aided Fixture Design (CAFD) is a essential task whose recognition will enable the integrated success of computer aided design (CAD). A fixture consists a base plate, locators, and clamps whose functions are to give the controlled work piece with a balance environment during a whole machining operation which includes setup and material removal. In the presented fixture used in GUKSS industries assembled all the parts one by one for welding via robot. During placing of angle more time is required by an operator and to clamp it as nut and bolt clamp is used to located on fixture. Next step, worker position three flat (one long and two short) and placing 32 rods in the slots. The nature of the slots are of V shape and rods are located in the slots one by one due to these reason the assembling time of product increases which is one of the key difficulty in current fixture. After welding thermal expansion takes places, due to which product get set in the fixture due to V shaped design.

2. DETAILS OF PAPER

1. EXPERIMENTAL SETUP: The vital principles of fixture design and the basic requirements of a fixture are reviewed in this section. The basic requirement of a fixture is to locate and secure the work piece in the required position and orientation, to assure repeatability. Thus, in the existing fixture no well suitable arrangement for assembling the rods is not seen properly. Due to which the assembling time of the raw material on the fixture is more. Number of clamps is more as on a single fixture in which two are nut & bolt clamp while four are toggle clamp. These results in increasing the production time and more fatigue of an operator. No regularity in the size and shape of the workpiece is seen due to which after placing the part on the fixture operator has to change the parts or has to rework it after operation for which time is loss. Thus, because of these problems, the rework cost, production time and labour effort are increased and also the desired quality is not obtained. The time calculations for different number of product on the previous fixture are measured in time variable .various time measurement are shown in table 3.1.

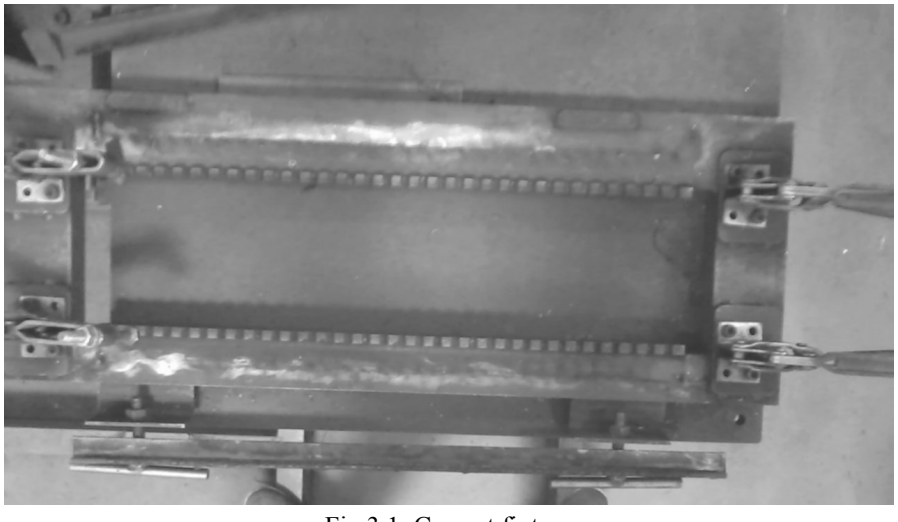

Fig 3.1. Current fixture

Table 3.1 Time measurement for Existing fixture.

No. of Readings / Components	1	2	3	4	5	6	7	8	9	10
Angle	11	9	13	12	9	10	14	15	15	**16**
Flat (short & long)	8	15	13	**16**	10	9	16	12	14	13
Rods	34	38	40	32	36	44	32	34	40	**45**
Adjustment	4	7	9	5	5	4	3	**10**	7	6
Setup	5	4	3	4	6	7	8	6	**9**	5
Clamp	7	9	5	6	**12**	10	12	7	9	10
Unclamp	3	5	4	6	**15**	9	10	8	7	11
Screw	3	5	8	7	3	6	8	7	10	**12**
Unloading	5	3	**6**	4	3	6	3	5	4	4
Total	**80**	**95**	**101**	**92**	**99**	**105**	**106**	**104**	**115**	**122**

2. WORKPIECE

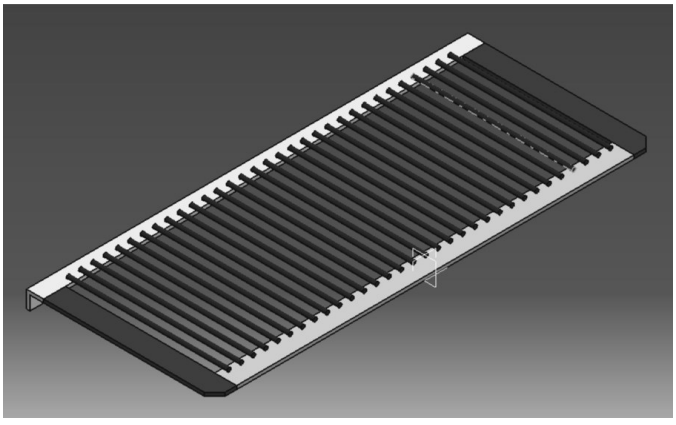

Figure 4.1 : Workpiece (Grid Frame)

The first subsection of the design case is workpiece. This subsection details all of the information about the workpiece. The first term is the name of the workpiece or the family name of the workpiece. This is to identify the workpiece and help group it into similar family of parts for easy retrieval. This subsection is further decomposed into workpiece detailed information of the different types that are usually welded are pipe, sheet metal, and bulk, varied. Another subsection of the workpiece is gathering information. This contains information on the number of parts as well as the gathering information. Contained within the gathering information is the number of parts and type of assembly operation. While both the number of parts and the type assembly operation are important this section also contains information about the parts. This subsection contains details about the CAD file.The last subsection under the workpiece is the numerical information. This contains the size, overall weight and the shape of the part. This subsection pertains to just the overall assembly, not its components.

3. EXPERIMENTAL METHODOLOGY: To solve the problem of the existing fixture, case based reasoning method has been applied which works on the principle of modification by taking into consideration of earlier solution (if any), retrieving the answer for it and adapting the solution for the current problem. Thus, by considering the modification and solution designing the fixture in the virtual environment of software. If the newly designed satisfies our need for the product with less time verify the solution and manufacture the fixture for taking into working and by storing the newly designed fixture data into the library for further retrieval.

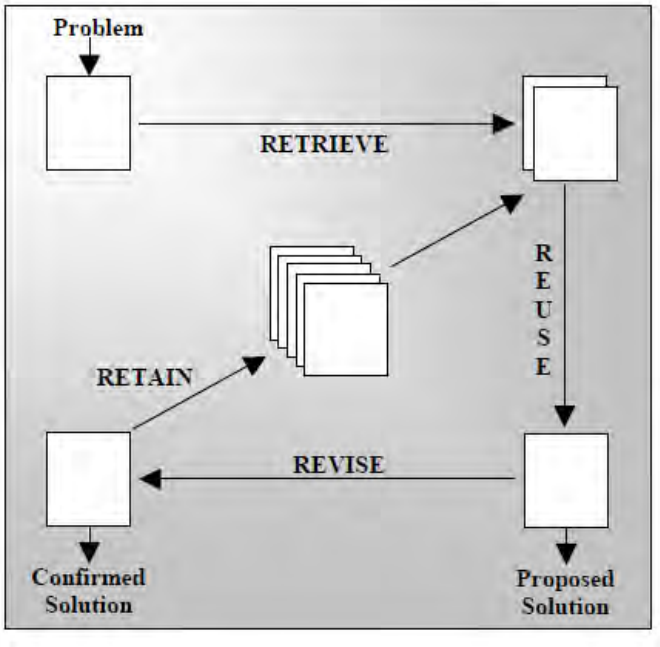

Fig.5.1 CBR cycle

In this experimental work, we have studied the current fixture and calculated various time on fixture. This study has given us the path to further designing. based on previous cases we have illustrate our first design of round shape slot fixture in which all 32 rods are rolling easily and capturing the locations. But after welding rods gets packed into the slots.

From illustration 1,we have retrieve the rolling parameter of rods but the design of slot has been changed from round to rectangular slots. In illustration 2, we have customized the round slots to rectangular slots which are shown in fig

2. Similarly in illustration 3,we have kept the rectangular slot as it is but by giving it radius as its edges have given us the better result then ill. 2. Thus by applying CBR method, we have modified the design by retrieving the parameter from the previous solution.

ILLUSTRATION 1: At initial stage, design of fixture is so designed depending on the rolling property of the rod which are collected like a bunch and are placed on the platform and are rolled to acquire there slot. As the level of rod is higher than all other parts, thus, two short flat ,one long flat and one angle are placed before on the fixture. The slot on the fixture is of round shape with a height of 5 mm.

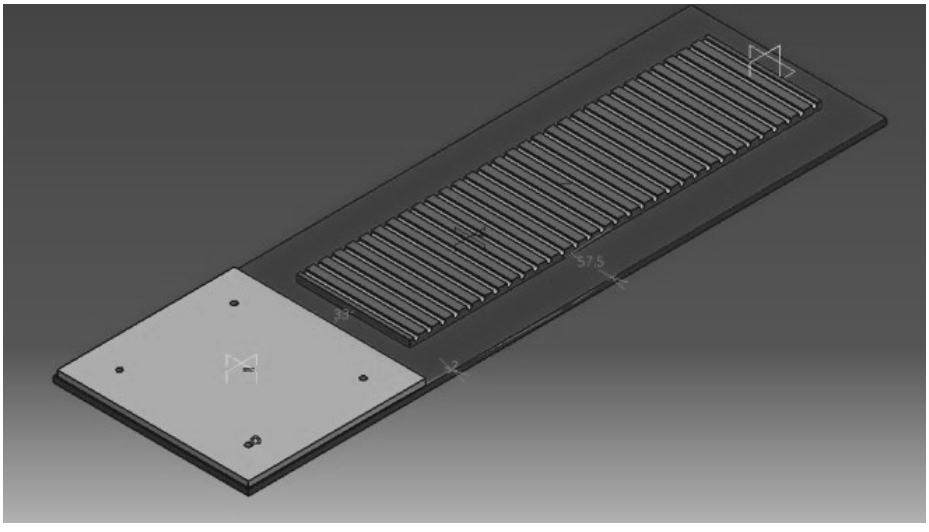

Fig 5.2. Round slot fixture.

During welding, the welding area gets expand due to heating because of which the dimension of rod also get increase a little which will be difficult for the operator to remove the welded product with more force reducing the efficiency of an operator. Due to these drawbacks further modification is carried out. Lastly, while manufacturing fixture it is typical to generate round slot on milling and time required for operations will also be more.

ILLUSTRATION 2: With the same rolling property of rods , as carried out in illustration 1the round shape of the slot is modified to rectangular slot which may take less operation time as compare to illustration 1 . The level of the platform plate and upper point of rod are same.

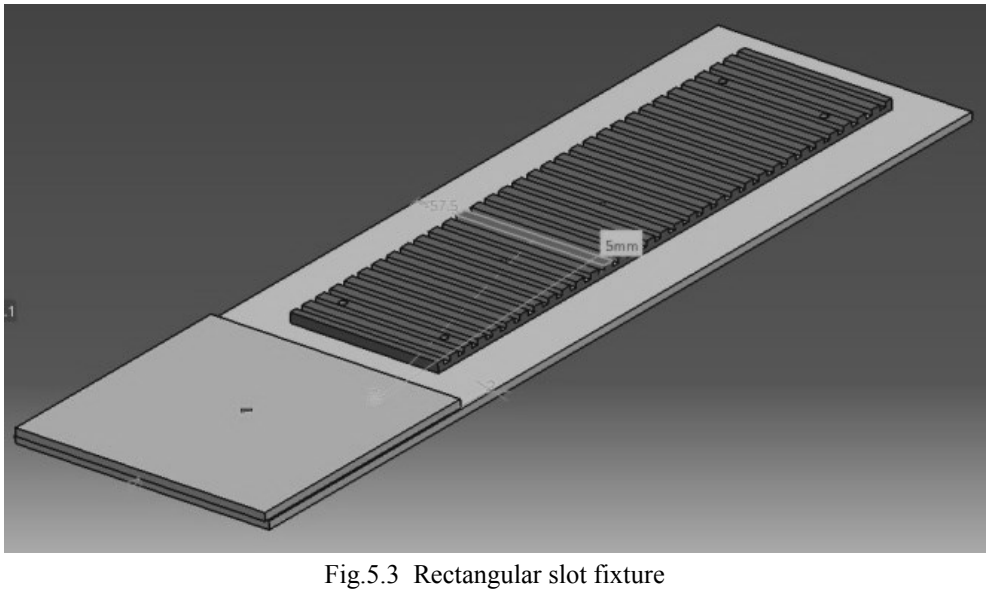

Fig.5.3 Rectangular slot fixture

Drawbacks of this fixture are 1) rod does not roll freely due to tapered edge.2) well dimensioned slot are not getting in milling operation.

ILLUSTRATION 3: Drawbacks of the illustration 2 are solved in this design. for making the rectangular slots ,channels are made by bending sheets. Due to which, radius is generated at the edge which will support the rod for easy rolling and the height of the channel is equal to the diameter of the rod which enables the rods for easy rolling. These small channels are then welded on a plate maintaining the the distance between two channels. The channels are so designed for fixture that welding is done from inner side due to cut off present at the corners.

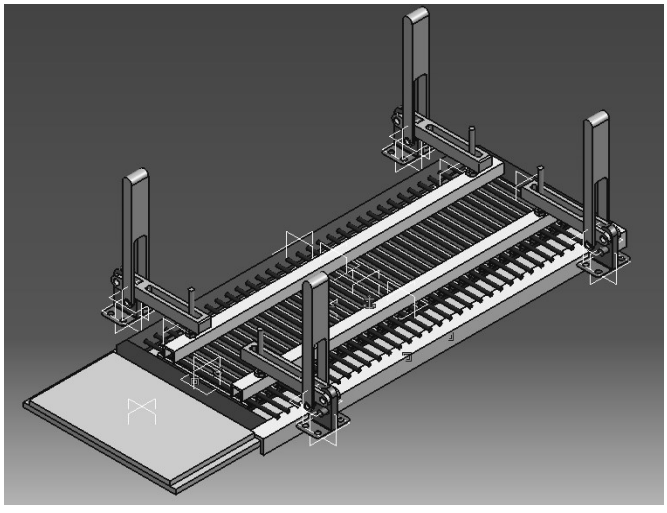

Fig. 5.4 rectangular slot fixture with radius

After the designed is confirmed, the next step is to place the clamp at proper positions. In the above image clamping position is same in current fixture. In this clamping position, time required by the operator to clamp and declamp takes more time.To reduce these time clamping position have been change and 4 toggle is replaced by 2 toggle with some adjustment. Figure 5.5 shows the assembly of fixture and product with clamping positions. Various design has been recommended for which time measurement is done on the finalized design which is shown in table 5.1

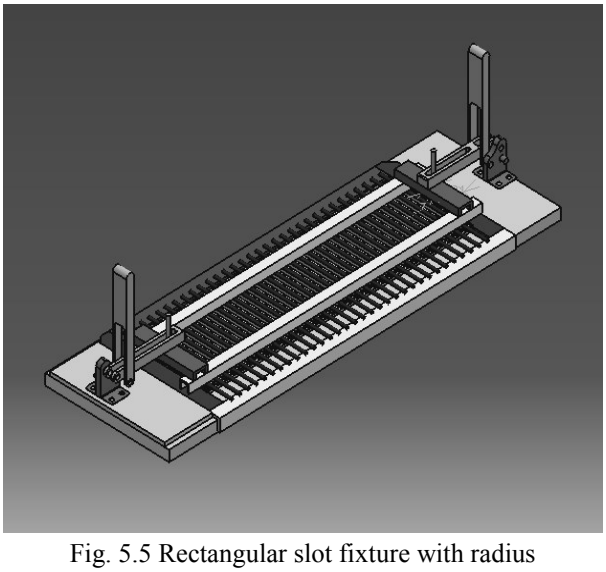

Fig. 5.5 Rectangular slot fixture with radius

Table 5.1. Time measurement for modified fixture.

No. of Readings / Components	1	2	3	4	5	6	7	8	9	10
Angle	6	8	7	**9**	6	8	8	7	6	7
Flat (short & long)	10	9	**16**	15	8	15	13	12	14	13
Rods	12	15	12	13	14	12	15	11	15	**16**
Adjustment	5	7	4	6	8	4	**9**	8	9	5
Setup	7	8	6	**9**	5	5	4	3	4	6
Clamp	5	4	4	**8**	7	5	6	4	5	6
Unclamp	6	4	5	7	5	**9**	4	4	6	8
Screw	5	3	4	**6**	5	4	4	5	6	6
Unloading	6	3	5	4	4	5	3	**7**	4	3
Total	**62**	**61**	**67**	**77**	**62**	**66**	**66**	**60**	**69**	**70**

3.CONCLUSION

This paper discuss the current approaches for supporting the fixture design.The CAFD approaches has been reviewed in terms of design phases and underlying technology on which it is based. The illustration 1 which was discussed has not given any major results as round slots are difficult to manufacture and required more force to remove the welded product from fixture. The round shape of the illustration 1 has been changed to rectangular slot in illustration 2 , but it was difficult to manufacture by milling operation.the illustration 3 has given the best result than both illustration 1 & 2. In this rods are simply rolled due to bending radius of the channel. The number of clamps are also reduced which cobines results into decreasing the assembling and clamping time.

The CBR methodology was applied to modify the fixture design by retrieving some parameters in the virtual environment of CATIA. It is possible to modified the fixture design by applying CBR method and make a new fixturing solution quickly by referring previous design cases.

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TECHNICAL ANALYSIS OF SECURITY INFRASTRUCTURE IN RFID TECHNOLOGY

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ABSTRACT

The paper is a technical analysis of the security infrastructure in the field of RFID technology. The paper briefly discusses the architecture of the RFID technology. Then it analyses the various features and advantages RFID technology has over the existing technologies like bar codes. This is followed by a discussion of the various disadvantages and security drawbacks of RFID technology that prevents its widespread adoption in the mainstream market. The paper concludes with a brief analysis of some of the security measures that are implemented within the RFID technology for securing up the whole infrastructure. The main aim of the paper is to focus on the drawbacks of the pre-existing security measures in RFID technology as well as to discuss the direction in which further research has to be carried out without the compromise on its unique features.

Keywords— *RFID, RFID tag, RFID reader, line of sight.*

1. INTRODUCTION

Radio Frequency Identification (RFID) technology is an information exchange technology using the radio frequency for transmission of information to and fro between the various places ([1], [2], [4], [21]). Such a technology is mainly implemented in the form of tags which contain information that can be read only by specific RFID tag readers. This technology has some distinct advantages over the existing information exchange mediums like bar codes in the form of wireless interaction between the RFID tags and readers. Moreover RFID technology supports a wider array of unique IDs in comparison to bar codes ([1]) as well as has a greater data retaining capacity. And the wireless interaction between the tag and the readers facilitates automatic assessment of product with minimal human interference.

2. OVERVIEW

In section 3, we briefly discuss the architecture of the RFID tags. In section 4 we discuss the applications and advantages of RFID technology. In section 5 we discuss the disadvantages and security drawbacks of RFID technology. We discuss some security measures that can be implemented within the RFID technical framework and in general for a more secure information transmission technology in section 6. We conclude the paper in section 7.

3. RFID ARCHITECTURE

The RFID technology is based on the transmission of data over electromagnetic fields (radio waves) ([4]). Here the information within the RFID tags is stored electronically. Based on the source of power derived by the RFID tags, they can be categorized mainly into two types ([25]):

- Active tags: These tags derive power from an external power source (In most cases, the RFID tag itself powers the active tags).
- Passive tags: These tags derive energy from within them and have a limited lifetime. The passive tags power the RFID tags through electromagnetic induction.
- A RFID tag consists of the following three parts ([9]):
- Antenna: It performs the function of receiving energy from external power sources as well as relay information to and fro between the tag and the reader.
- Semi-conductor chip attached to antenna: It co-ordinates with the antenna in the exchange of information between the tag and the reader.
- Encapsulation: It acts as protective layer to the antenna and the semi-conductor chip from external environment.

A RFID tag always works in conjunction with a reader. The reader electromagnetically induces power in the tags as well as communicates with the antenna of the RFID tag.

4. APPLICATIONS AND ADVANTAGES OF RFID TECHNOLOGY

Radio frequency identification technology serves as a prerequisite in IoT and it has multi-dimensional applications within the real world. The facilitation of wireless interaction between RFID tags and other electronic devices leads to ease of interaction and exchange of digital information. Some of the most prominent uses and advantages of RFID technology are as follows:

- RFID in the transportation sector:
  - (a) RFID tags can be employed in car services for storing identification numbers of vehicles along with other information which can then be used for performing automatic inventories using static RFID readers appropriately placed at various locations such as parking lots, exits of garage etc. ([37], [44])
  - (b) In the airline industry, RFID tags can be used for efficient categorization of baggage based on routing location. This will lead to automated routing of the baggage with minimal error and a huge deduction in losses incurred due to misrouting or loss of baggage ([30], [46], [47]). However, such RFID tags can only be employed in conjunction with static RFID readers placed at conveyor belts ([9]).
  - (c) RFID tags can be used as re-usable tickets for public transportation systems. Such use will facilitate online purchasing or in this case online re-activation of the RFID tags for use of transportation as well as implementation of real time passenger information system ([7]).
  - (d) RFID tags and readers can be implemented for the operation of automated electronic tolling system ([38], [40]).

- RFID in the health sector:
  - (a) RFID tags can be assigned to patients containing their health information. Moreover such an implementation along with the installation of static RFID tags in the vicinity can help in proper and timely administration of the patients' meal and other medications along with maintenance of a medical database of the patients' health progress, allergies to various foods and medicines, the various drugs administered against the respective ailments etc.
  - (b) RFID tags attached to medicine bottles can contain the medicinal information about the drug. Along with the use of various sensor technologies, RFID tags can also be used to determine the level of content within the bottle and appropriately facilitate alerts to users and online purchases for replenishment of content by exchange of information over the internet.

- RFID in hotel industry:
  - (a) RFID tags in the form of smart cards are being used in the modern hotels replacing the keys to each room for enhanced security and convenience of the customers.

- RFID in Retail Industry and advantages of RFID over Bar Codes:
  - (a) RFID tags are automatically read by RFID readers in vicinity leading to reduction in manual labor and an enhanced and proactive real time tracking of products.

(b) As against bar codes, no line-of-sight is required between RFID tags and readers for reading of information ([3]).

(c) RFID tags offer higher reading rates of contained information in comparison to bar codes ([14]).

(d) RFID tags can be re-written with new information and as such are re-usable and updatable with new information about the products to which they are attached to.

(e) RFID has a much greater data capacity than a bar code.

(f) Item attached with RFID tags can be tracked in real-time point-to-point automatically thus reducing the involvement of manual labor as well as economic expenditure and time ([10]).

(g) RFID tagged items can be securely stored in the appropriate place as the tags can be programmed accordingly to send out notifications when the items leaves a specific place without proper clearance ([8]).

(h) The real time tracking facilitation by the RFID tags attached to products leads to better prediction of a particular product in the market.

(i) The RFID tags can be programmed to alert the retailers when a particular product has to be replenished in the market to prevent the "out of stock" situation as well as to prevent the loss of customers when the demand is high due to non-availability of the products.

- RFID technology in security

(a) In some countries the passports are being attached with RFID tags for prevention of theft and forgery ([18], [28], [31], [34]).

(b) RFID technology is being rapidly implemented in the agricultural and livestock farming field for automated tracking of livestock as well as proper financial assessment against the livestock based on their presence or loss from the farmhouses ([6], [11], [22]).

(c) Being embedded with anti-cloning technology ([41], [43], [49]), the RFID cards prove to be more secure than the magnetic strips.

(d) RFID cards works when present in the vicinity of the card reader without the need of direct line of sight or direct contact like swiping.

5. DISADVANTAGES AND SECURITY DRAWBACKS OF RFID

The slow rate adoption of the RFID technology in the mass market even after the presence of a huge number of advantages clearly points that this technology is not yet ready for such a wide spread adoption due to a number of limiting factors. Some of the most prominent drawbacks of this technology are as follows:

i. The RFID technology proves to be unreliable in mediums like metals or liquids where RFID tags fails to be read.

ii. RFID technology, in spite of its higher reliability than electromagnetic strips and bar codes, is yet to be perfected as a significant percentage of the RFID tag fails to function properly.

iii. RFID tags can suffer from orientation problems as sometimes these tags do not interact with the readers when both are misaligned with respect to each other.

iv. The non-adoption of line of sight technology of the bar code leads to a major security drawback in parallel to its ease of use. The use of high gain antenna by a competitor can lead to loss of confidential information of products attached with RFID tags as the information contained within these tags can be easily picked up by such antennas.

v. RFID technology comes with some major financial drawback as for the use of RFID tags; a particular adopter has to first install RFID reader(s) and computer networks for assessing the information in the RFID tags. This leads to an expensive installation cost and as such a technology proves to be futile from an economic perspective.

vi. RFID technology has a signal threshold just like in the cellular communication field below which RFID technology becomes non-functioning. Moreover such a technology may malfunction in areas with high signal interference.

vii. After reading a large number of RFID tags, it may so happen in rare cases that the reader sometimes administers tag which does not exist thus leading to an error in the database entry. Such a problem is known as Ghost Tag problem in RFID.

viii. The facilitation of automated environment in the work place by the adoption of RFID tags in the various sectors of an industry like library management of assets, verification at checkouts etc. leads to decreasing demand of human workforce which leads to widespread unemployment in a region.

ix. RFID tags are susceptible to removal from an object with ease.

x. Interference between tags placed within $.125^{th}$ of an inch from each other can take place.

6. SECURITY MEASURES

Some of the most prominent security measures that are being adopted till now for securing up the whole RFID security infrastructure are as follows:

- To counter the problem of Ghost Tags in RFID tags, verification technologies like CRC can be implemented in any of the three items mentioned below:
  - (a) RFID tag
  - (b) Tag reader
  - (c) Data from the tag.

- The problem arising due to misalignment of the RFID tags with respect to the reader can be solved through the implementation of the following two solutions:
  - (a) Tags having multiple axis antennas.
  - (b) Multiple readers
- Physical locking of information in the RFID tags at the cost of rewriting capabilities of the tags will ensure proof of origins of the tags.
- RFID tags can be encrypted with an author's own private key. In this way an author can write information into the tag memory along with the following three security information:
  - (a) Author's name
  - (b) Reference to the author's public key
  - (c) Algorithm used in non-encryption form.

This method helps in verifying whether the data in the tag memory has gone through any modification without the author's consent. However one of the drawbacks of this security measure is that for updating the information within the tag's memory, a key management system is required for the management of the private key.

- RFID tags can be protected from leak of information in the presence of third party high gain antenna by enclosing the tags inside a Faraday Cage ([23], [13]) during transit.
- Selective active jamming of RF signals can prevent the theft of RFID tag information ([13], [15], [27]).
- RFID tags, if used for wireless payment, should be followed by some additional steps for verification of the user such as codes sent to cellular devices, fingerprint verification etc. This is known as multifactor authentication ([26], [33])
- Implementation of read detectors will help in detection of unauthorized readers in the vicinity ([24]).
- To avoid the misreading of tags by the RFID readers, tags can be designed to respond to frequencies set by the readers. It can also prevent leakage of information by the frequent change of frequencies by the RFID readers.
- With advances made in the direction of integration of RFID with wireless sensor networks ([17]), it becomes imminent to implement the security measures of wireless sensor networks ([5], [12], [36], [42], [45], [48]) for securing up the RFID technology. As such implementation of sleep deprivation attack detection systems ([20]), implementation of TinySec ([19]), dynamic reconfiguration of wireless sensor network ([16]) and various other intrusion detection systems ([39]) becomes necessary for securing up the RFID technology when working in conjunction with wireless sensor networks.

7. CONCLUSION

Radio Frequency Identification technology, over its many cutting edge features and advantages, still has a long way to go for mainstream adoption due to its several drawbacks in terms of security. Adoption of security measures by compromising its re-writable feature or any of its other features brings down the whole technology to the level of the existing technologies like bar code and in the same way retaining the various features of RFID at the cost of its security makes the technology less favorable for adoption in the market. As such development of specific measures which addresses its security drawback without compromising its various features should be pushed forward for a sustainable future of this technology on the mainstream market. In addition to the development of such new security measures, the adoption of the existing data hiding techniques ([29], [32], [35]) during transmission of information can contribute to a more secure info exchange between the RFID tag and the authorized reader.

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DESIGN AND SIMULATION OF PID TUNING TECHNIQUES WITH FLC SYSTEM

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ABSTRACT

In this paper the new methodology for designing of PID controller is presented.PID controller are the most widely used controller in the industry. Tuning of a PID controller is an important task for obtaining the desired closed loop specifications (settling time, maximum overshoot and steady state error).There are many methods proposed for the tuning of PID controller out of which Ziegler Nichols method is the most effective conventional method.

This paper presents different PID tuning formulas for a third order process. They are based on the knowledge of the ultimate gain, ultimate period. The main focus of this project is to apply soft computing techniques that are fuzzy logic to design & tuning of PID controller to get better dynamic & static performance at the output.

Keywords: - *Fuzzy logic controller, MATLAB simulation, PID controller, Ziegler Nichols tuning Method.*

1. INTRODUCTION

The quality of control in a system depends on settling time, rise time and overshoot values. The main problem is to optimally reduce such timing parameters, avoiding undesirable overshoot and longer settling times to solve this problem; many authors have proposed different approaches. A first approach is the Proportional Integral Derivative (PID) controller application. They are extensively used in industrial process control application [1]. PID controller has three principle control effects. The proportional (P) action gives a change in the input (manipulated variable) directly proportional to the error signal. The integral (I) action gives a change in the input proportional to the integral of error, and its main purpose is to eliminate offset. Whereas the derivative (D) action is used to speed up the response or to stabilize the system and it gives a change in the input proportional to the derivative of the error signal. The overall controller output is the sum of the contributions from these three terms. The general form of the PID controller is given below in equation (1).

$$u(t) = K_p\, e(t) + \frac{1}{T_i}\int_0^t e(t)dt + T_d\,\frac{de(t)}{dt} \qquad (1)$$

Fig. 1 shows that PID controller structure in parallel form which is more flexible than series form.

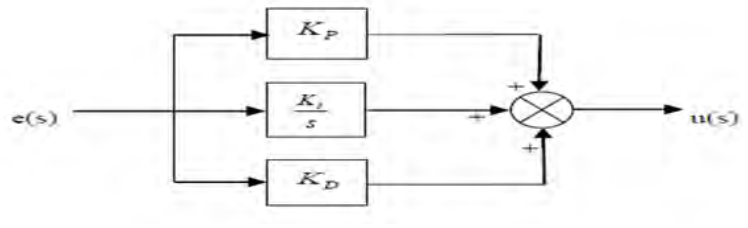

Fig.1 PID controller structure

Where u(s) and e(s) denote the control and the error signals, respectively, and proportional gain (K_P) integral time (T_I) and derivative time (T_D) are the parameters to be tuned. The goal of PID controller tuning is to determine parameters that meets the closed loop system performance specifications. In this paper various PID tuning formulas for a third order process has been analyzed, based on the knowledge of ultimate gain, ultimate period.

2. PROBLEM FORMULATION

PID controller consists of Proportional, Integral and Derivative gains. The closed loop control system is illustrated in Fig.2 Where *r*, *e*, *y* are respectively the reference, error and controlled variables.

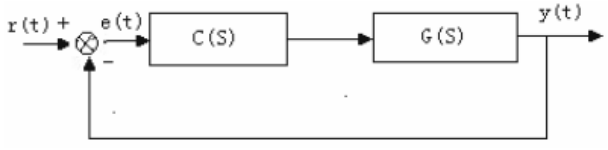

Fig.2 Closed loop control system

In the diagram of Fig.2, G(s) is the plant transfer function and C(s) is the PID controller transfer function that is given as:

$$C(s) = K_p + \frac{K_i}{s} + K_d s$$

Where K_p ,K_i, K_d are respectively the proportional, integral, derivative gains/parameters of the PID controllers that are going to be tuned. The plant used here is a DC motor model which is a third order system written as [2]

$$G(s) = \frac{Y(s)}{U(s)} = \frac{1}{S^3 + 9S^2 + 23S + 15} \qquad (2)$$

The close loop response of the system gives $M_p = 0$ & $T_s = 4.12$(sec)

3. TUNING METHODS

Tuning of a controller is a method of determining the parameters of a PID controller for a given system. A PID controller is described by three parameters; K_P , T_i and T_d. The necessity of tuning of the parameter of PID controller is very important. Ziegler –Nichols method is one of the mostly used tuning methods of PID controller.

4. ZIEGLER NICHOLS TUNING METHOD

The most popular tuning methodology was proposed by Ziegler and Nichols in 1942 [1]. The closed-loop tuning method requires the determination of the ultimate gain (K_u) and ultimate period (P_u). This can be achieved by adjusting the controller gain till the system undergoes sustained oscillations at the ultimate gain or critical gain (K_u), while maintaining the integral time constant at infinity and the derivative time constant at zero. The Ziegler-Nichols tuning method is based on the determination of process inherent characteristics such as the process gain, process time constant and process dead time. These characteristics are used to determine the controller tuning parameters.

By applying Z-N Method the step response of the K_p=192 & P_u=2 is shown in fig 3.

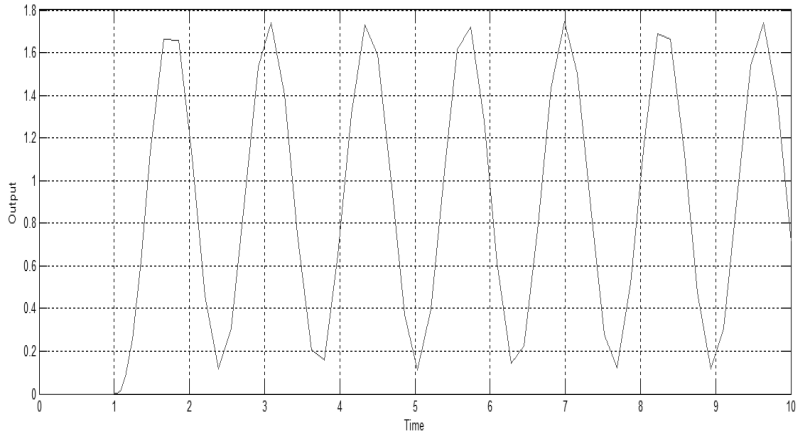

Fig.3. Step response of K_p=192

Table 1. Tuning parameters for Ziegler Nichols closed loop Ultimate gain method

Type of controller	Parameter		
	K_p	T_i	T_d
PID Controller	$0.6K_u$	$P_u/1.2$	$P_u/8$

As per Table 1, $K_P = 115.2$, $K_i = 1/T_i = 0.6$ and $K_d = 0.25$, With the above values of K_P, K_i and K_d, step response is shown in Fig.4. $M_p = 18.7\%$, $t_s = 2.65$ sec, $e_{ss} = 0$.

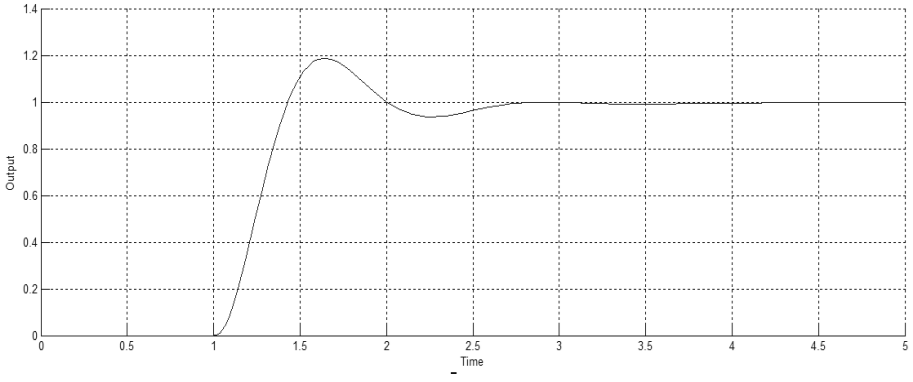

Fig.4 Unit step response for $K_P = 115.2$, $K_i = 0.6$ & $K_d = 0.25$

5. FUZZY LOGIC CONTROLLER

Fuzzy Logic was initiated in 1965[3] by Lotfi A. Zadeh , professor for computer science at the University of California in Berkeley. Basically, Fuzzy Logic (FL) is a multivalued logic that allows intermediate values to be defined between conventional evaluations like true/false, yes/no, high/low, etc. Fuzzy control provides a formal methodology for representing, manipulating and implementing a human's heuristic knowledge about how to control a system. The fuzzy controller block diagram is given in Figure 5, where we show a fuzzy controller embedded in a closed-loop control system. The plant outputs are denoted by $y(t)$, its inputs are denoted by $u(t)$, and the reference input to the fuzzy controller is denoted by $r(t)$.

The fuzzy controller has four main components

- The "rule-base" holds the knowledge, in the form of a set of rules, of how best to control the system.
- The inference mechanism evaluates which control rules are relevant at the current time and then decides what the input to the plant should be.
- The fuzzification interface simply modifies the inputs so that they can be interpreted and compared to the rules in the rule-base. And
- The defuzzification interface converts the conclusions reached by the inference mechanism into the inputs to the plant.

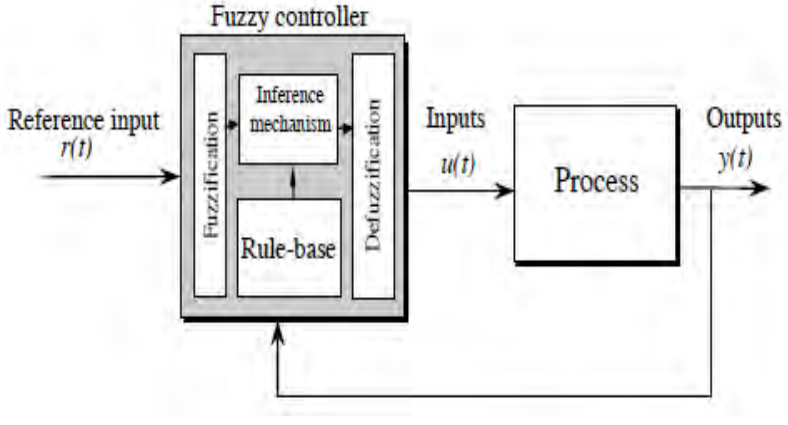

Fig.5.Blocks of fuzzy controller

6. DESIGN OF FLC WITH MATLAB

Simulink model of the fuzzy controller and the considered process with unity feedback is shown in Fig.6.

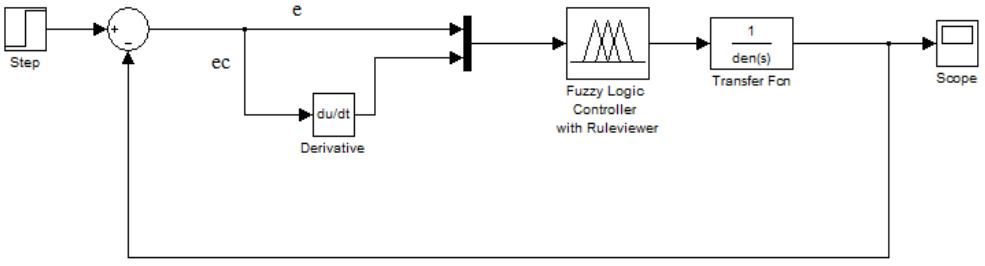

Figure 6: Process with FLC

For a two input fuzzy controller, 3,5,7,9 or 11 membership functions for each input are mostly used[4].In this paper, only three fuzzy membership functions are used for the two inputs error 'e' and derivative of error 'ec' as shown in Figure. 7,8 & 9. The fuzzy membership functions for the output parameter 'U' are shown in Fig. 10.

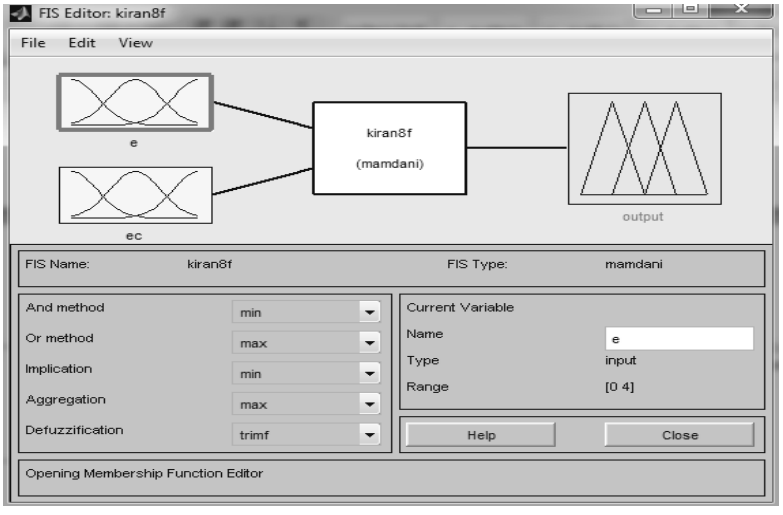

Figure 7: Mamdani Fuzzy system

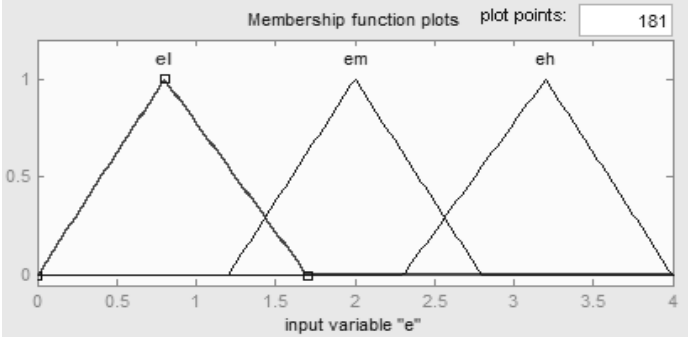

Figure 8: Membership functions for inputs ‘e’

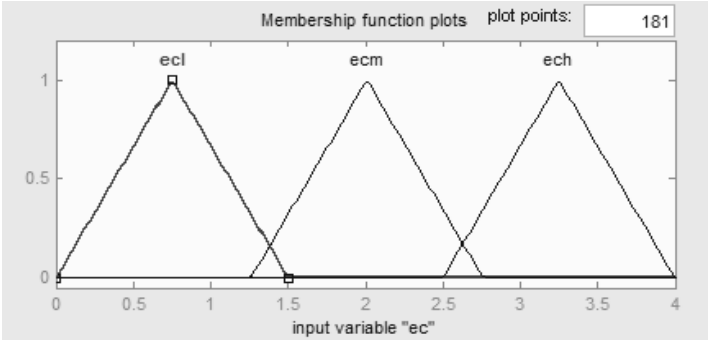

Figure 9: Membership functions for inputs ‘ec’

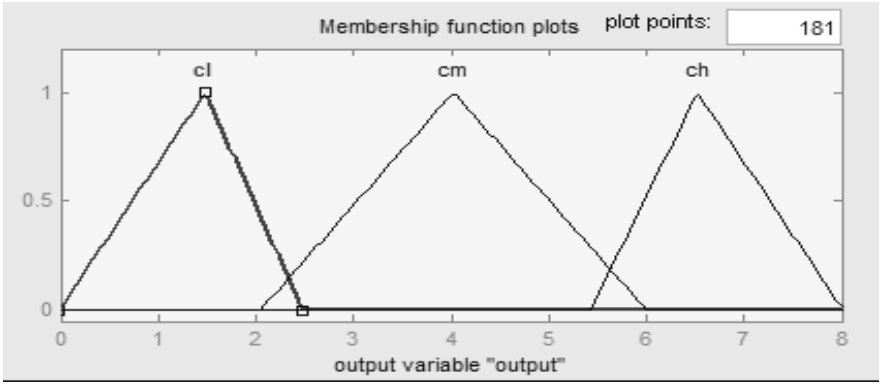

Figure 10: Membership functions for output 'U'

Basically a linguistic controller contains rules in the if-then format, but they can be presented in different formats. In many systems, the rules are presented to the end-user in a format similar to the one below.

- If error is ‘el’ and change in error is ‘ecl’ then output is ‘cl’.
- If error is ‘el’ and change in error is ‘ecm’ then output is ‘cm’.
- If error is ‘el’ and change in error is ‘ech’ then output is ‘cm’.
- If error is ‘em’ and change in error is ‘ecl’ then output is ‘cl’.
- If error is ‘em’ and change in error is ‘ecm’ then output is ‘cm’
- If error is ‘em’ and change in error is ‘ech’ then output is ‘ch’
- If error is ‘eh’ and change in error is ‘ecl’ then output is ‘cm’.
- If error is ‘eh’ and change in error is ‘ecm’ then output is ‘cm’.
- If error is ‘eh’ and change in error is ‘ech’ then output is ‘ch’.

Table.2. Meaning of the linguistic variables in the Fuzzy Inference System

el	error low
em	error medium
eh	error high
ecl	error control low
ecm	error control medium
ech	error control high
cl	control low
cm	Control medium
ch	Control high

Step response of the controlled third order process by using fuzzy logic system is shown fig.11.

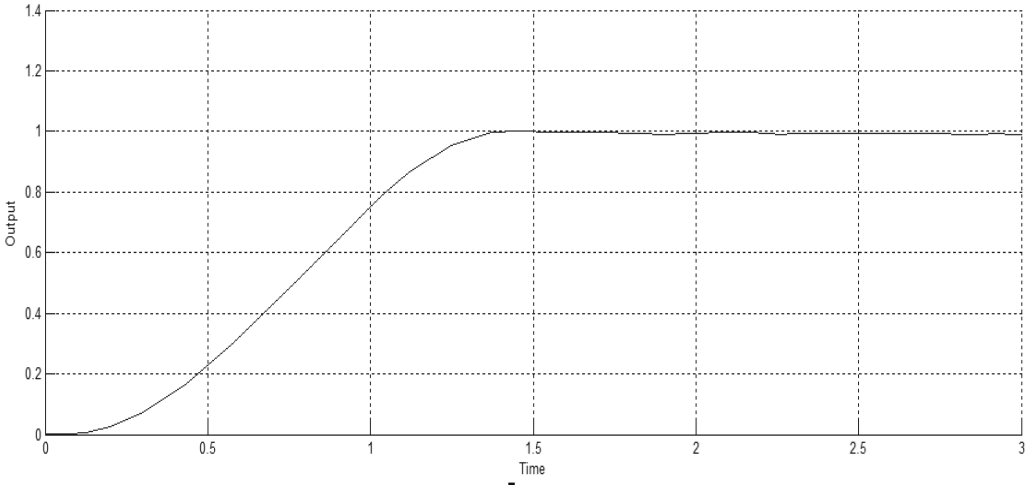

Figure 11. System response with FLC

In fig.11 shows that maximum overshoot (M_p) = 0% & settling time(t_s)= 1.4 sec, e_{ss} = 0.

7. CONCLUSION

In this paper, two different methods regarding the tuning at conventional PID and fuzzy logic controller has been presented. Ziegler Nichols method gives the approximate value of any response not the appropriate or exact value and it is having one more disadvantage that the Maximum overshoot and settling time will be more. For better performance to reduce the settling and rise time for getting better response. To get the better performance it is necessary to reduce both the Maximum overshoot and settling time simultaneously and for this purpose Fuzzy logic technique can be used. These techniques will successfully eliminate the whole overshoot from the output response. The designed controllers are simulated through the MATLAB.The results obtained from different tuning methods are shown in the table given below.

Table 3. Comparison of different PID tuning methods on time response specification

Controller	**Time domain performances Parameter**		
Used	M_p(%)	T_s(sec)	E_{ss}(%)
Close loop system	0	4.12	0
Z-N Method	18.7	2.65	0
FLC	0	1.4	0

The simulation results shows that compared to the traditional PID controller techniques , fuzzy self-tuning PID controller has a better dynamic response curve, shorter response time, small overshoot, high steady precision, good static and dynamic performance.

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OPTIMIZATION OF GATING SYSTEM FOR REDUCING THE DEFECTS IN DIVETER WHEEL USING MOLD FLOW SOFTWARE:A CASE STUDY

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ABSTRACT

The objective of this research was to optimize gating/riser system based on CAD and simulation technology with the goal of improving casting quality such as reducing incomplete filling area, decreasing large porosity and increasing yield. Hence this paper deals with thecomputer assisted casting simulation techniques which are used to analyze the gating related and methoding related defects in green sand casting. Shrinkage porosity analysis was performed using casting simulation technique by introduction of a newgating system designed, solid model developed for single cavities mould. Number of iterations using casting simulation software wasperformed for mould filling and solidification analysis, to reduce the level and intensities of shrinkage porosities in cast component. With new gating and feeding system design reduction in shrinkage porosity (about 20%) and improvement in yield (about 9%) has been observed.

Keywords—*Casting simulation optimization; Casting Defects, Mold Filling solidification analysis*

1. INTRODUCTION

Casting is oldest process of making complex shapes of metal materials in mass production. Now a daysfoundry industries in developing countries suffer from poor quality and productivity due to involvement of number of process parameters in casting process. Even if we control all the process parameter in manufacturing, defects in casting are observed and hence casting process is also known as process of uncertainty which challenges explanation about the cause of casting defects[1].Casting defects analysis is the process of finding the root cause of occurrence of defects in the rejection of casting and taking necessary steps to reduce the defects and to improve the casting yield [2].

Hence there is a need for the development of a computer-aided casting process design tool with CAD, simulation, and optimization functions to ensure the quality of casting. The objective of the research presented in this paper was to optimize gating/riser systems based on CAD and simulation technology with the goal of improving casting quality such as reducing incomplete filling area, decreasing large porosity and increasing yield. In this paper, a CAD and simulation technology based optimization framework is presented. Given a CADmodel of part design and after its being converted to casting model, the first objective is to evaluate cast-ability of the casting design. From given part design, CAD model has developed which further converted into casting model to evaluate the castability of casting design.

2. METHODOLOGY

In this method of casting defect analysis, Computer aided casting simulation technique is used for methoding, filling and solidification related defects such as shrinkage porosity, hot tears, etc. Flow chart of proposed method of casting defect analysis has shown in figure 1

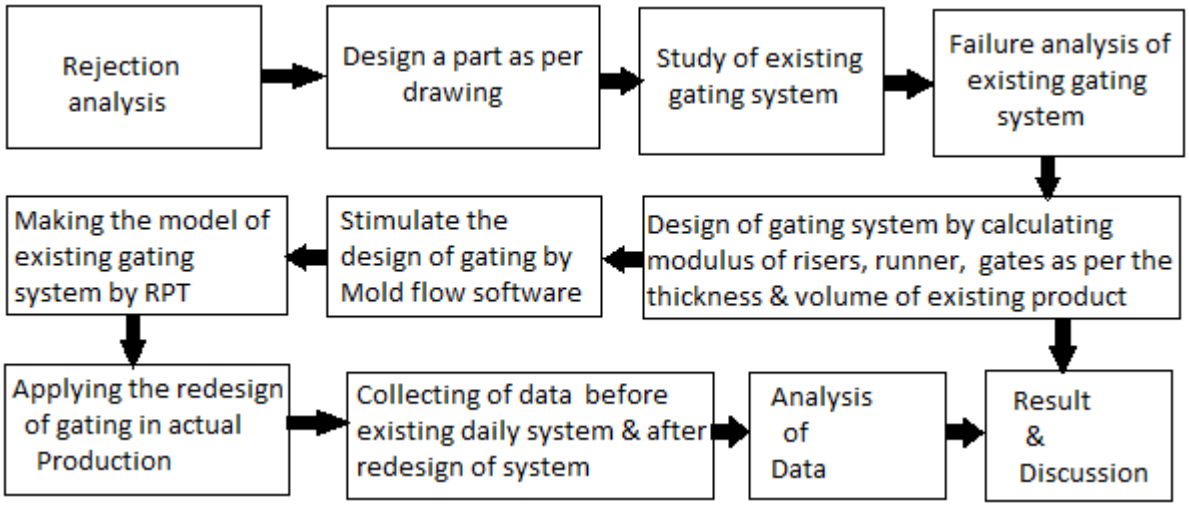

Figure 1: Flow chart of casting defects analysis and casting simulation technique

Methodology used to achieve optimize process parameters;

- Select any defect observed because of existing gating system
- Set the target to achieve lower casting defect by adjusting gating system or replacing it by new gating system.
- To minimize temperature loss during mould filling and minimize oxidation.
- Producing casting with minimum defects.

3. CASTING SIMULATION FOR CASTING DEFECTS ANALYSIS

Simulation is the process of imitating a real phenomenon using a set of mathematical equations implemented in a computer program. In casting simulation the mould filling and solidification analysis is done by using an algorithm or program based on finite volume method, to identify the hot spots and hence defects like shrinkage porosities, hot tears, cracks, etc**.** The simulation programs are based on finite element analysis of 3D models of castings and involve sophisticated functions for user interface, computation and display. The casting model (with feeders and gates) has to be created using a solid modeling system and imported into the simulation program [4]. Ravi [5] has suggested casting simulation and optimization methodology as shown in Figure 2.

Part model, Material, Method design, Process parameters, Existing defects	STEP 1. Data Gathering……
Parting line, cores, feeders, feedaids, gating system, mold cavity layout	STEP2 Method Design……
Model import, Mesh generation, Material and process, computation, visualization	STEP 3. Simulation……
Modify design, Simulation, Check quality, check yield, Check cost	STEP 4. Optimization…….
Method report, Analysis report, Images slides, Compare results, Archive project	STEP 5. Project Closure…….

Figure 2: Casting simulation-optimization methodology

4. EXPERIMENTAL WORK

Experiments were performed in a small scale ferrous foundry producing cast iron & ductile iron cast component.

After carrying out rejection analysis it was found that in cast component named ‘Diverter wheel’ the rejection was maximum 20-25% due to gating related defects like shrinkage, blow hole and gas porosity etc. This defects commonly observed on middle and outer periphery of the Diverter wheel. Hence diverter wheel was selected as a component for defect shrinkage analysis by casting simulation technique. As a explained above after doing rejection analysis, the component named Diverter wheel, the rejection was found to be maximum up to 20-25 %. Due to gating related defects like shrinkage, blow holes and gas porosity etc.

4.1 ANALYSIS OF SHRINKAGE OF DIVERTER WHEEL BY CASTING SIMULATION TECHNIQUE Casting simulation technique can be efficiently used for analysis of casting defects related to methoding such as shrinkage porosities

by the mold filling and solidification analysis. There are five distinct stages in casting simulation projects; Data collection, method design, numerical simulation, method optimization, and project conclusion. The casting simulation and optimization methodology is shown in figure 2 and thevarious steps involved are discussed below.

The data related to the diverter wheel such as existing defects, process parameters, materials, casting yield, feeding yield, gating yield, pouring temperature and methods design was collected and analyzed as shown in table 1.Existing images of diverter wheel with defect is shown in figure 3. The input required for the simulation program is .STL file which has been prepared from CAD model of casting. The CAD model for diverter wheel is shown in figure 4.

Table 1. Numerical result of existing gating system

	Existing gating
Casting yield	68.34 %
Feeding yield	71.69%
Gating yield	93.80 %
Pouring time	9.04 sec

Figure 3: Shrinkage defects observed on casting

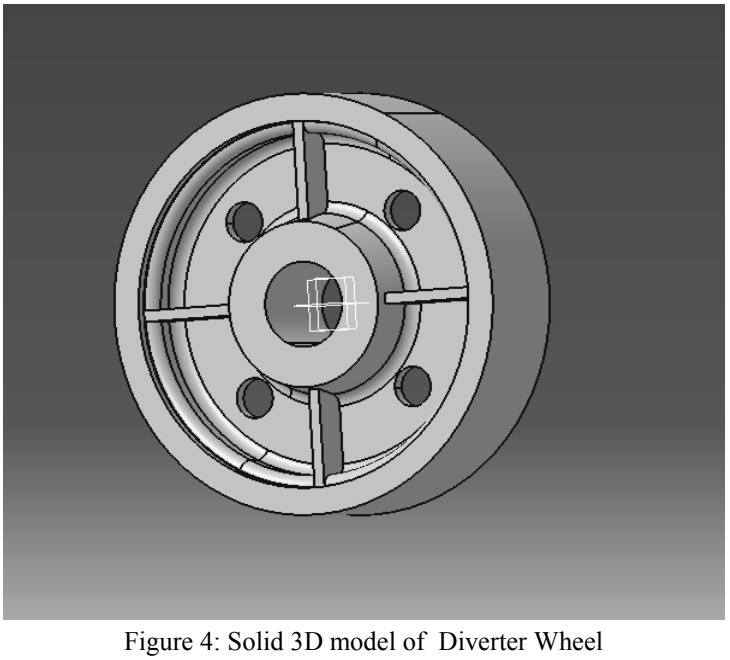

Figure 4: Solid 3D model of Diverter Wheel

4.2 METHOD DESIGN In existing methoding, shown in figure 5, four side feeder was used to pour as well as feed the casting, during solidification of single cavities mold. During studying of existing gating system, it was found that Feeder was not feeding the casting properly which results in shrinkage porosities occurs outside as well as inner portion of the casting shown in Figure3.

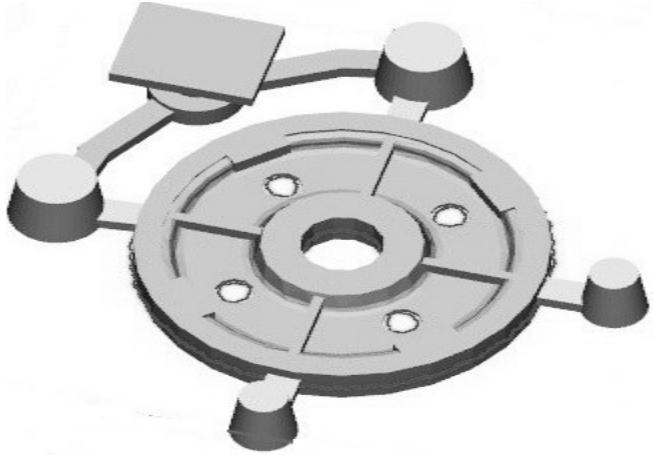

Figure 5: Existing gating system

In this stage a gating system was designed (for single cavity mold)using theoretical formulae used for gating and risering system design. Risering was designed by modulus method and technician's experience. Four side feeders with appropriate sizes were used to feed the single cavities mould as shown in Figure 5.

Feeder yield- The volume of the feeder must be minimized to increase the yield. The criterion is given by;

$C_{f3} = N_c V_c / (N_c V_c + \sum_i V_{fi})$ ……Eq. (1)

The feeding yield is calculated using equation 1 and shown in Table 5.

Gating yield- The volume of the gating system must be minimized to increase the yield. The criterion is given by;

$C_{G4} = N_c V_c/(N_c V_c + V_g)$ ……Eq. (2)

The gating yield is calculated using equation 2 and shown in Table 5.

Casting yield- The volume of casting system must be minimized to increase the yield. The criterion is given by;

$C_{c5} = NcVc/(NcVc+\sum_i V_{fi}+Vg)$ ……Eq. (3)

The casting yield is calculated using equation 3 and shown in Table 2.

Where, Nc is the number of casting cavities per mold, Vc is the volume of each cavity, and V_{fi} is the volume of feeder. Vg is the volume of common gating system for all cavities in the mold.

Table 2. Numerical result of proposed gating system

	Proposed gating
Casting yield	77.44 %
Feeding yield	77.44 %
Gating yield	95.11 %
Pouring yield	9.50 sec

4.3 OPTIMIZATION AND SIMULATION In this paper, casting simulation softwareAutoCast (courtesy: IIT Bombay, India) wasused for mold filling and solidification analysis. At the initial stage, the gating and risering system for the single cavities of the mold was designed as shown in Figure5. In this gating system, two neck was provided to casting to fill the mold cavity. Pouring is through centralsprue and neckare attached to the feeder. The yield with this iteration was found to be 68%.

Simulation for mold filling and solidification analysis with existing gating system severe shrinkage porosities at outer portion and inner portion of the casting was obtained shown in figure 6.

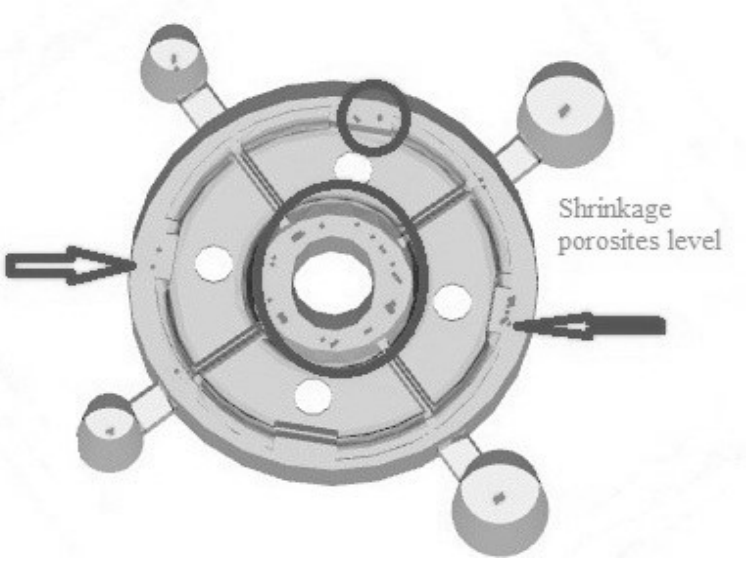

Figure 6: Shrinkage porosities level existing feeder

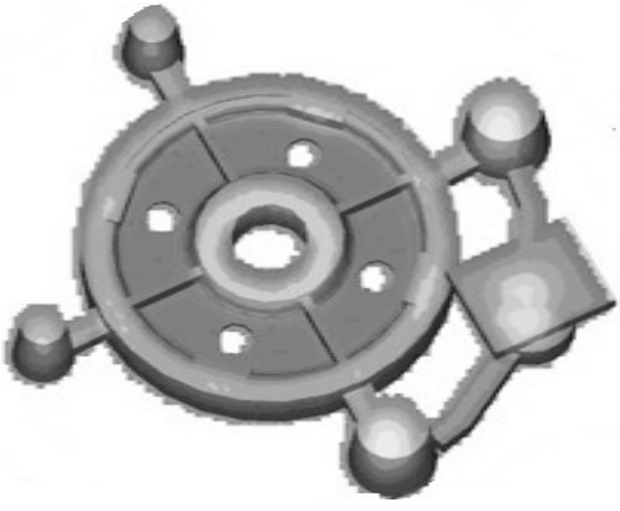

Figure 7: Liquid-solid conversion of existing gating system

Hence, to minimize the shrinkage porosities, blow hole and gas porosityetc, number of repeated performance for gating system design of Diverter wheel was performed and optimum design for gating system was selected. In new optimum methoding, two feeder of optimum size was used for single cavities and one was primary feeder which was slightly bigger than the other which is known as secondary feeder. The secondary feeder feeds the material if the primary feeder fails to feeds the molten metal or if the molten metal is not reached to all location.The new optimum Design of feeder is shown in figure 8.

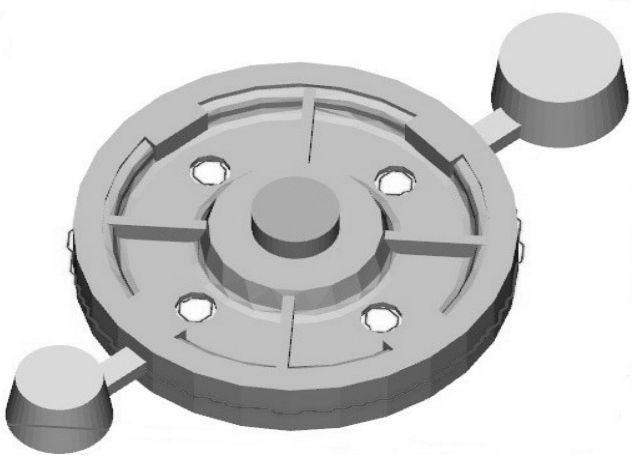

Figure 8: New design of feeder system

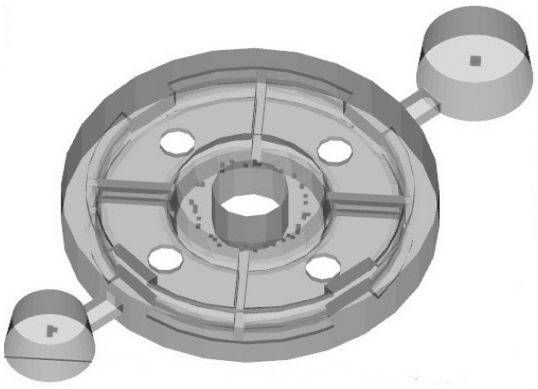

Figure 9: Shrinkage porosities level of suggested feeder

Due to changes in gating system, the shrinkage porosity was considerably reduced as compared to existing gating system, in which it was shifted to feeder which was clearly shown in figure 9.

Figure 10 shows the final gating system for single cavities Diverter wheel with two Optimize feeder , Runner bar, Gates, Core, Pouring basin etc.

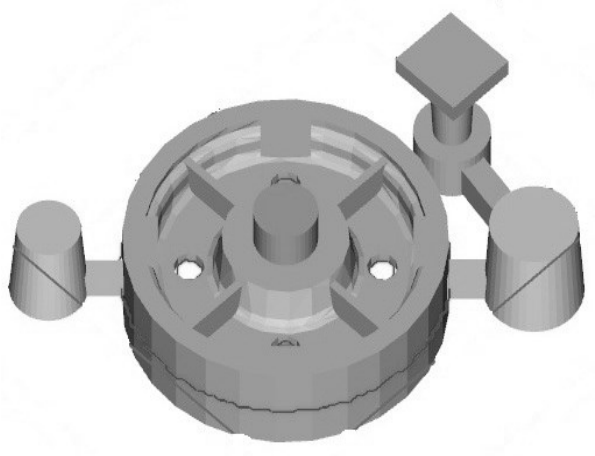

Figure 10 : New gating system

Finally, Optimum Method of gating system design for Diverter wheel with single cavities mold was implemented and it was found that rejection of cating due to shrinkage porosities was reduced by 20% as compared to previous gating system.

Figure 7 shows that Simulation results for shrinkage porosities with optimum iteration. Due ti this gating system design the shrinkage porosity was considerably reduced up to acceptable level for casting as compared to the iteration of stage I(compare Figure 9 and 6). Figure11 shows Liquid-solid conversion of new gating system and feeder works satisfactorily and results in sufficient feeding of casting during solidification and hence reduction in level of shrinkage porosities inside the casting. With this methoding (optimum iteration) the yield was 77 %observed which is more than theexisting methoding used in foundry. The data related to casting yield, feeding yield, gating yield and pouring temperature of existing gating and proposed gating has been taken from shown in table 3.

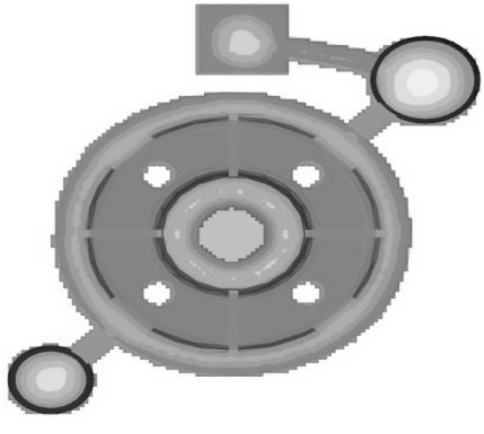

Figure 11: Liquid-Solid conversion result of proposed gating system

Table 3. Simulation result of existing gating & proposed gating system

	Existing gating	Proposed gating
Casting yield	68.2 %	77.5 %
Feeding yield	71.11 %	80.90%
Gating yield	93 %	95 %
Pouring time	4.7 sec	7.8 sec

5. CONCLUSION

- A new method of casting defect analysis was proposed and studied which has computer aided casting simulation technique for analysis of rejection of casting due to defects related to sand, molding, methoding, filling and solidification in green sand casting.
- From above experimentation it has been observed that in existing gating system the casting yield, feeding yield & gating yield was roughly 68.27%, 71.54% & 93.86%. In proposed gating system it was improved by 77.52%, 80.72% & 95.14%. Due to this there is saving in material about 9%.
- Two feeder of optimize size was used instead of four feeder which was used in old gating system. Due to the poor design of existing gating system, shrinkage, blow hole & gas porosity was observed on casting. All these defects were completely removed and hence quality of casting is improved.
- By using casting simulation method the % rejection of casting due to gating related defects has been reduced from 20% to approximately 3%.
- For analysis of defect like shrinkage porosities computer aided casting simulation technique is the most efficient and accurate method. The quality and yield of the casting can be efficiently improved by computer assisted casting simulation technique in shortest possible time and without carrying out the actual trials on foundry shop floor.
- A proper gating/feeder system is very important to secure good quality of green sand casting through providing a homogenous mold filling pattern
- By comparing the simulation result of optimized casting model with the original model, it can be conclude that the defects decreased by nearly 20% and the yield increased by approximately 9%.
- The application of computer aided methoding, solid modeling, and casting simulation technologies in foundries can able to minimize non value added time in casting development.

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PHYSICAL AND NUMERICAL MODELING OF AN ORIFICE SPILLWAY

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ABSTRACT

As a part of the design process for hydro-electric generating stations, hydraulic engineers typically conduct some form of model testing. The desired outcome from the testing can vary considerably depending on the specific situation, but often characteristics such as velocity patterns, discharge rating curves, water surface profiles, and pressures at various locations are measured. Due to recent advances in computational power and numerical techniques, it is now possible to obtain much of this information through numerical modeling. Computational fluid dynamics (CFD) is a type of numerical modeling that is used to solve problems involving fluid flow. Since CFD can provide a faster and more economical solution than physical modeling, hydraulic engineers are interested in verifying the capability of CFD software. Although some literature shows successful comparisons between CFD and physical modeling, a more comprehensive study would provide the required confidence to use numerical modeling for design purposes. This study has examined the ability of the commercial CFD software Fluent to model a variety of spillway configurations by making data comparisons to both new and old physical model experimental data.

Key Words : Spillways, Pressure, Simulation, Numerical models.

1. INTRODUCTION

Background Physical scale modeling has been used in the design and investigation of hydraulic structures for over 100 years. The design process has typically involved the development of a preliminary design on the basis of theoretical and empirical methods. A physical scale model of this arrangement would then be constructed in two- or three-dimensions and various scenarios run to confirm whether the hydraulic performance was acceptable and to extract data for input to the design. The methods are tried and tested and the outputs from the model testing in terms of data and observations are invaluable in the design process. However, the construction, operation, and testing of physical models is often a time-consuming and expensive exercise. Furthermore, the modification of the model to trial alternative arrangements or to optimise features can add weeks to a testing programme.

Through recent advances in computing power and modeling software capabilities, it is now feasible to undertake complex three-dimensional analyses using CFD techniques. To date, CFD modeling has generally been used as a valuable tool in the optimisation phase of the project prior to the commissioning of a physical model study. The major benefit of the CFD modeling in this capacity was that it allowed the early identification of problematic flow features and modifications to the layout could be trialled rapidly and cost-effectively. Although CFD modeling packages now have the capability to analyse complex hydraulic conditions common in spillways such as air entrainment, flow separation, turbulence and shock waves, there is however a significant lack of calibration and validation studies (between CFD and physical models and also between model and prototype) for these advanced applications and caution should be applied to their use in design [6].

OBJECTIVES

1. To model the complex flow pattern of two phase turbulence flow in spillway by the numerical model
2. To expand the simulation results from numerical models to large scale physical models to ensure proper simulation of flow in complex multiphase flow.
3. Validate the results of numerical modeling with experimental results.
4. Try to establish the use of CFD models in physical model studies as a complementary tool.

SCOPE OF STUDY The present study is to model the complex flow pattern of two-phase turbulence flow in spillways by using the numerical model. The numerical model is suggested to expand the simulation results from numerical models to large scale physical models to ensure proper simulation of flow in complex multiphase flows. Due to recent advances in computational power and numerical techniques, it is now possible to obtain much of this information through numerical modeling.

The assumption of the complex turbulence flow in spillways is the flow would be two phase free surface flow without any large or observable suspended sediment that can affect the flow pattern. The simulation results from numerical models are compared to the large scale physical models to ensure proper simulation of flow in complex multiphase flows [1].

Computational fluid dynamics (CFD) is a type of numerical modeling that is used to solve problems involving fluid flow. Since CFD can provide a faster and more economical solution than physical modeling, hydraulic engineers are interested in verifying the capability of CFD software [4].

Computational fluid dynamics (CFD), have been in use for years but recent advancement in computer technology has made CFD software commercially available. Therefore this study has been initiated to use this tool for solving hydraulic model case study.

The desired outcome from the testing can vary considerably depending on the specific situation, but often characteristics such as velocity patterns, discharge rating curves, water surface profiles, and pressures at various locations are measured [3]. Some literature shows successful comparisons between CFD and physical modeling, a more comprehensive study would provide the required confidence to use numerical modeling for design purposes.

2. PHYSICAL MODEL USED IN THE PRESENT STUDY

PHYSICAL MODEL SETUP A 2-D sectional model was constructed to a geometrically similar scale of 1:50 with transparent Perspex sheets in a glass sided flume. One full span and two full piers with breastwall and ski-jump bucket were incorporated in the model. Piezometers were provided along the centre of span and side of pier for hydrostatic pressure measurement. Piezometers were also provided along the centre line of the bottom of breastwall profile. Necessary arrangements were made for measurement of discharge, pressures, velocities and water levels.

3. NUMERICAL MODELING

Physical models play a major role in evolving the design of hydraulic structures like spillways and energy dissipators. Some scale effects are associated with the physical models for modeling of air water flows. Numerical modeling has been sparsely used in this field due to the complex nature of the flow. However, with the advancement of the computing facility Computational Fluid Dynamic (CFD) modeling is being increasingly used in simulation of spillway flows. Simulation of flow over the spillway is possible with advanced CFD software as two phase air-water flow can be modelled [1].

The Navier–Stokes equations can describe virtually any flow problem. However, they are the most difficult to solve. In the last two decades, simulation techniques based on the Navier–Stokes equations have been applied to a large number of flow problems with suitable assumptions and approximations. The rapid development in the computer technology has made the computational fluid dynamics an effective and economical tool for solving various problems in Fluid Mechanics [4].

Computational Fluid Dynamics is a branch of science, which deals with replacing the differential equations governing the fluid flow, into set of algebraic equations. Theses algebraic equations are solved with the help of digital computers. CFD can be a very useful tool to minimize the efforts and expenses of physical modeling as it consumes less time and gives accurate results once the CFD model is validated. It provides good control over all the flow (geometric and dynamic) parameters. It is also cost effective. However, one cannot replace the physical model at this stage, since the validation of the CFD model is done using the results of the physical model.

TURBULENCE MODEL There are three major approaches to predict turbulent flows, viz. Statistical Turbulence Modeling (STM), Large Eddy Simulation (LES) and Direct Numerical Simulation (DNS). Statistical turbulence models based on the Reynolds- Averaged Navier-Stokes (RANS) equations represent transport equations for the mean flow

quantities only, with all the scales of the turbulence being modelled. There are many turbulence models available.

Among the linear turbulence models, the widely used two-equation model is based on:

- The turbulent kinetic energy equation k and
- The turbulent eddy dissipation, ε , or the turbulent frequency ω .

The Renormalisation group k-ε, turbulence models were chosen in the present study to simulate the flow over orifice spillways.

BOUNDARY AND INITIAL CONDITIONS Boundary conditions are the most important and critical aspects of the numerical modeling [3]. Utmost care has to be taken in the formulation of boundary conditions so that the physical phenomenon could be represented satisfactorily. It is important that the boundary conditions accurately represent what is physically occurring for a given flow condition. Boundary conditions specify the flow variables or their gradients on the boundaries of computational flow domain.

UPSTREAM BOUNDARY CONDITION The upstream boundary can be set up at a flow inlet at which the reservoir water level but the incoming discharge and/or velocity are unknown. This section should be far away from the spillway to avoid the reflection effect.

DOWNSTREAM BOUNDARY CONDITION The downstream boundary should be located based on the range of the interested domain [2]. For the study of the spillway crest and the aerator region, the downstream condition will have no effect on the upstream flow since the flow over the downstream slope of the spillway is supercritical. However, the downstream section has to be chosen far downstream of the end of the spillway so that the ski jump jet/hydraulic jump is fully formed.

SOLID BOUNDARY CONDITION The interface between the fluid and solid boundary is considered as closed boundary. It is also called as wall boundary. There are three kinds of solid boundary conditions:

- Full slip boundary condition
- Partial slip boundary condition and
- No slip boundary condition

The full slip means that tangential velocity at the inner grid is equal to tangential velocity on the solid surface; while no slip means tangential velocity on the solid surface is zero; for partial slip condition, a wall function should be used. There is no flow across solid boundaries. Selection of the three alternatives depends on the nature of governing equations, relative magnitude of the grid size and the boundary layer thickness in the flow domain.

INITIAL CONDITION Before starting the solution, an initial guess has to be provided for the solution flow field. An accurately assumed velocity and free surface profile will accelerate the convergence of the computations.

OPERATING CONDITIONS Operating pressure is defined at the atmospheric pressure. The operating density is specified as 1.223 m3/s, as air was the primary phase out of the two phases viz. air and water

The various processes involved in formulation of problem, as follow :

- Create the geometry and grid
- Start the appropriate solver for 2-D or 3-D modeling
- Import the grid (case)
- Check the grid
- Select the solver formulation
- Choose the basic equation to be solved i.e. turbulent
- Specify material properties
- Specify the boundary conditions
- Adjust the solution control parameters
- Initialise the flow field
- Compute the solution
- Examine the results
- Save the results

4. RESULTS AND DISCUSSION

Hydraulic model studies on the original design were conducted to assess

- Discharging capacity of the spillway
- Pressure Profiles

- Water surface Profile and
- Suitability of the geometry of the profiles

1) DISCHARGING CAPACITY OF THE SPILLWAY

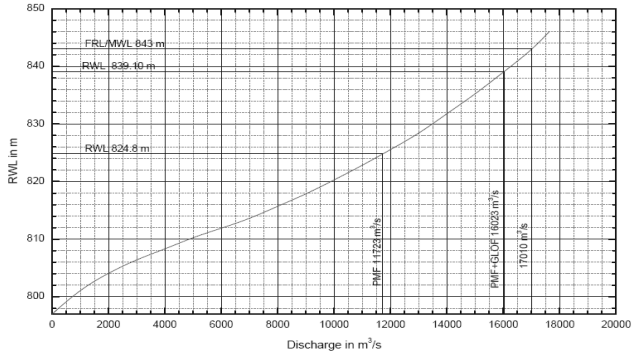

Figure 1 Discharging Capacity Curve

PRESSURES ON THE SPILLWAY PROFILE Comparison of pressure profile is more important for assessment of cavitation potential of the flow. Results of both hydraulic and numerical modeling were superimposed. The general trend and the magnitude were in good agreement with the observed data on the physical model. Some variations were seen which were probably due to local mesh geometry or error in measurement on physical modeling. The pressure or cavitation indices could only be calculated at selected locations in physical model where Piezometers were provided. However, the same could be calculated at closely spaced points in numerical model. Thus, a continuous profiles for pressure could be generated which indicate the zones which are susceptible to cavitation damage.

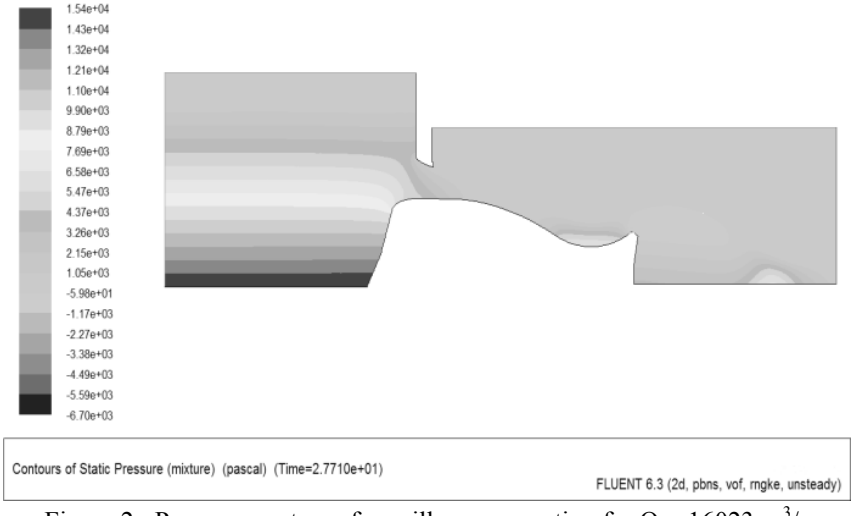

Figure 2 : Pressure contours for spillways operating for Q = 16023 m^3/s

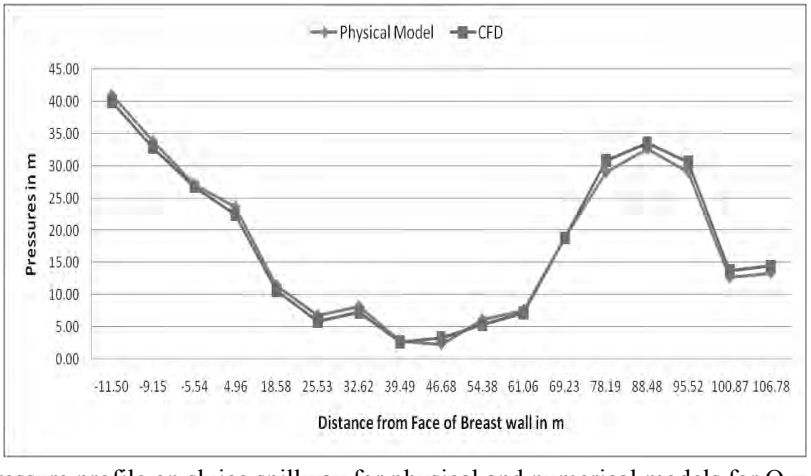

Figure 3: Pressure profile on sluice spillway for physical and numerical models for Q = 16023 m^3/s

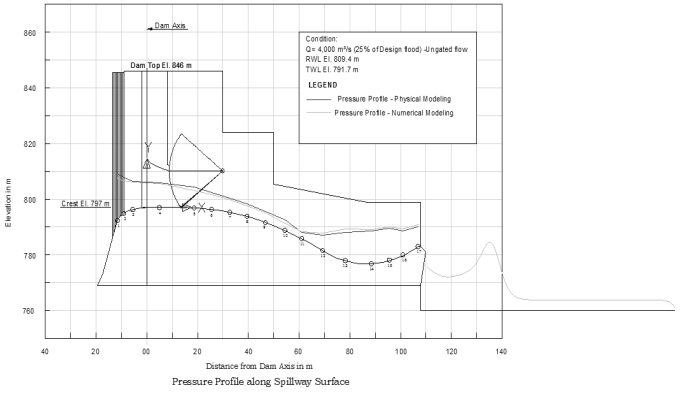

Figure 4: Pressure profile on sluice spillway for physical and numerical models for Q = 4006 m^3/s

WATER PROFILE OVER THE SPILLWAY Water surface profiles are desired in order to determine appropriate heights of training and divide wall and obtaining reservoir water levels such that overtopping does not occur. To numerically solve the rapidly varying flow over spillway, it is important that the free surface be accurately tracked.

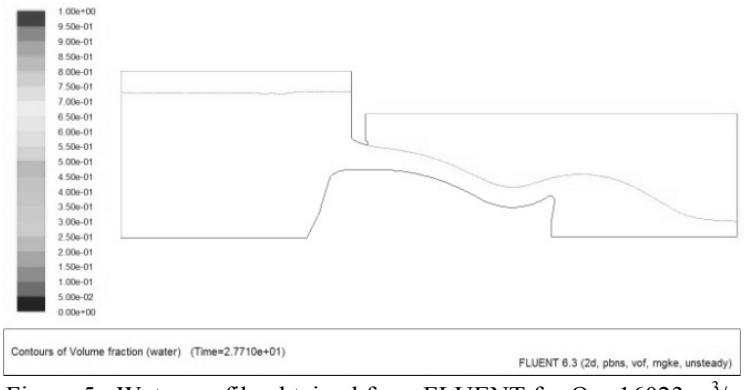

Figure 5 : Water profile obtained from FLUENT for Q = 16023 m^3/s

5. SUMMARY & CONCLUSION

CONCLUSIONS – PHYSICAL MODEL STUDIES Studies were carried out on 1:55 scale 2-d sectional model. The conclusions from these studies are as follows :

- The discharge of 17010 m^3/s could be passed at FRL El. 843 m, with all 7 spans operating fully open. This is about 6% more than the design discharge of 16023 m^3/s. It was observed that design discharge 16023 m^3/s could be passed passed at reservoir water level El. 839.1 m through all 7 spans fully open. As such, discharging capacity of the spillway is considered to be adequate [5].
- The upper nappe of jet issuing from the sluice opening was seen adhering to the breastwall bottom profile for the orifice regime thus making the entire height of orifice fully effective for ungated operations of spillway [5].
- The trunnion axis of the radial gates is well above the water surface for all the discharges [5].
- Water was spilling over the training wall intermittently for discharges 8000 m^3/s and above due to high TWL. The height of training wall may be suitably designed based on the water surface profiles, bulking of flow due to air entrainment in prototype and free board requirement. However there is no need of increasing the height of divide walls [5].
- The hydrostatic pressure distributions on the spillway profile and breastwall bottom profile are acceptable [5].
- The performance of the ski-jump bucket was not satisfactory for entire range of discharges for gated and ungated operation of spillway as the bucket lip was getting submerged to the extent of 8.6 m to 20 m for discharges of 4006 m^3/s to design discharges of 16023 m^3/s due to high tail water levels. Submerged ski action with aerated surface rollers riding over the bottom jet could be seen in the bucket. Ski-jump bucket was susceptible to TWL as hydraulic jumo was seen forming in the bucket for slight increase in tail water levels [5].
- It is suggested that the design of the bucket may be modified by raising the bucket lip by about 3 to 4 m so as to reduce the submergence depth due to tail water to improve the performance of Ski-jump bucket [5].

Physical model studies play very important role in finalizing hydraulic efficient design. But it is very time consuming and difficult to accommodate these changes and conduct experiments for each modification and get the results.

The results of numerical simulation of the final adopted design gave the encouraging results with reference to the physical modeling. This shows the ability of CFD to simulate the complex flow phenomenon.

CONCLUSIONS – NUMERICAL MODEL STUDIES The final adopted design is simulated using numerical model. The ability of the CFD software FLUENT to model spillway flow behaviour proved to be quite successful. In general, it seems that FLUENT can accomplishment nearly the same results as a set of physical model experiments. The following conclusions can be drawn from this study:

- FLUENT can successfully model a spillway's water surface profile for a variety of discharge conditions as compared to physical model testing. The general trend of physical model water profiles can be achieved using computational fluid dynamics.
- The general trend of physical model pressure profiles can be achieved using computational fluid dynamics.

As demonstrated in studies, the numerical model can be used efficiently as a complementary tool to physical model studies for investigation of flows over spillways, thus obviating the necessity of studying several alternatives on the physical model involving time and cost. This study shows that, numerical tools like CFD codes are quite convenient to calculate the water and pressure profile over the spillway. The analysis for pressure profile shows 2% to 50% relative difference in the physical and numerical model readings. The high relative difference was due to very low pressure magnitude where small difference makes huge relative difference. For discharges and water profile the relative difference is of the order of 1% to 5 %. CFD gives an insight into flow patterns that are difficult, expensive or impossible to study using traditional physical modeling techniques. Although physical model studies may be more expensive and time consuming than computational modeling, they are still crucial for providing data for numerical model calibration and validation studies. The unique combination of computational expertise in physical flow modeling can be applied in concerned to provide cost effective, practical solutions to spillway flow problems. Thus, CFD modeling can be used as a complementary tool along with physical modeling to solve complex flow problems of spillways.

6. ACKNOWLEDGEMENTS

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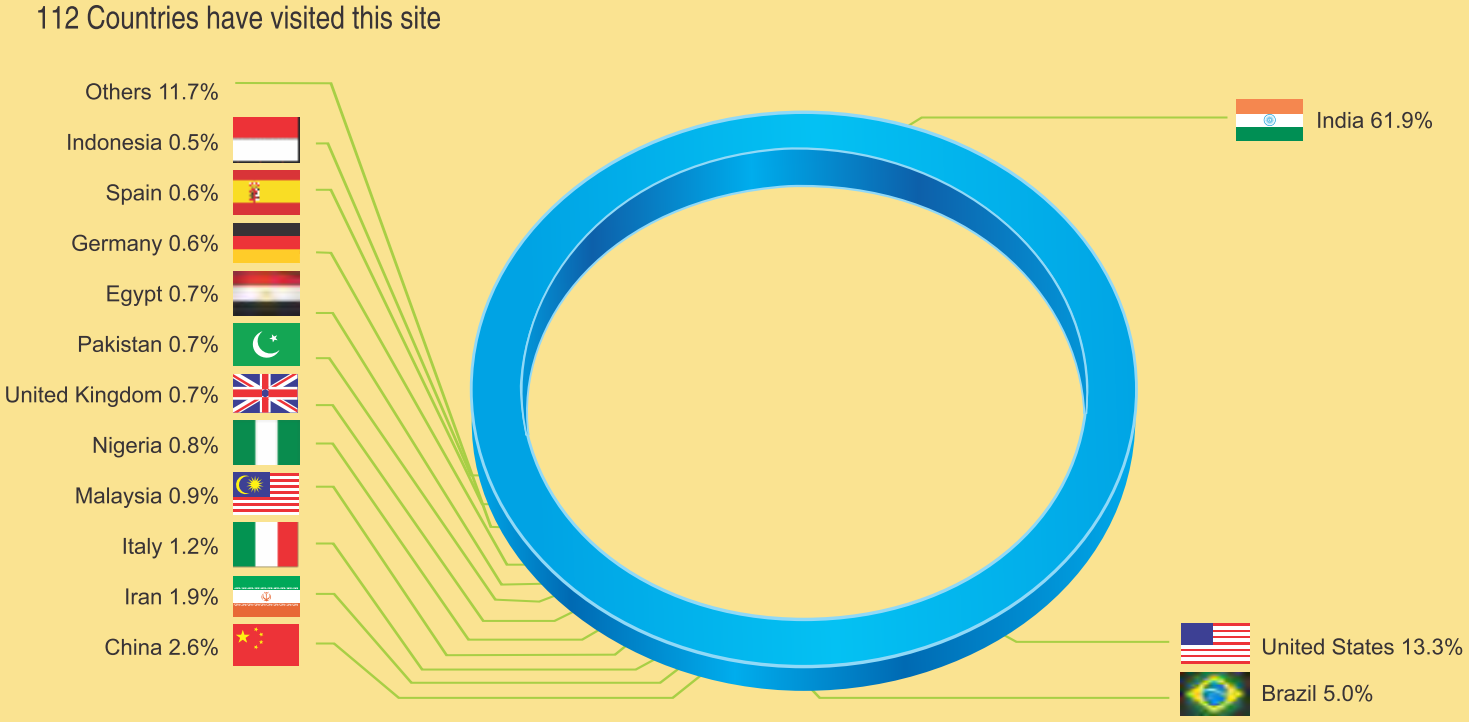

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