VLSI - B.Tech Project's

S.NO	PROJECT TITLE
1	A New VLSI Architecture of Parallel Multiplier–Accumulator Based on Radix-2 Modified Booth Algorithm. (Verilog)
2	An Efficient Architecture for 3-D Discrete Wavelet Transform. (Verilog)
3	The Design of FIR Filter Base on Improved DA Algorithm and its FPGA Implementation. (Verilog)
4	Design of On-Chip Bus with OCP Interface. (Verilog)
5	Design of a Self-Motivated Arbitration Scheme for the Multilayer AHB Bus matrix. (Verilog)
6	Low Complexity and Fast Computation for Recursive MDCT and IMDCT Algorithms
7	An Efficient Architecture for 2-D Lifting-based Discrete Wavelet Transform. (Verilog)
8	Power-Efficient Pipelined Reconfigurable Fixed-Width Baugh-Wooley Multipliers
9	A Spurious-Power Suppression Technique for Multimedia/DSP Applications(Verilog)
10	Design of AES (Advanced Encryption Standard) Encryption and Decryption Algorithm with 128-bits Key Length (VHDL)
11	DDR3 based lookup circuit for high-performance network processing. (Verilog)
12	Multiplication Acceleration Through Twin Precision
13	32-bit RISC CPU Based on MIPS (VHDL)
14	High Speed Hardware Implementation of 1D DCT/IDCT (Verilog)
15	Efficient FPGA implementation of convolution
16	High Speed VLSI Architecture for General Linear Feedback Shift Register (LFSR) Structures
17	Implementation of a visible Watermarking in a secure still digital Camera using VLSI design
18	Implementation of FFT/IFFT Blocks for OFDM

S.NO	PROJECT TITLE
19	Design and Implementation of Efficient Systolic Array Architecture for DWT (Discrete Wavelet Transform) (Verilog)
20	Design and Implementation of 10/100 Mbps (Mega bits per second) Ethernet Switch for Network applications (Verilog)
21	Design and Implementation of USB 2.0 Transceiver Macro-cell Interface (UTMI) (VHDL)
22	A Versatile Multimedia Functional Unit Design Using the Spurious Power Suppression Technique (Verilog) (Same as 9th Project)
23	Design and Implementation of Digital low power base band processor for RFID Tags (Verilog)
24	Design and Implementation of Reversible Watermarking for JPEG2000 Standard
25	FPGA Implementation of 3D Discrete Wavelet Transform for Real-Time Medical Imaging (Same as 3D-DWT – no 2 project)
26	Design and Implementation of High Speed DDR SDRAM (Dual Data Rate Synchronously Dynamic RAM) Controller (VHDL)
27	Design and Implementation of Lossless DWT/IDWT for Medical Images
28	High Performance Complex Number Multiplier Using Booth-Wallace Algorithm
29	High Speed Parallel CRC Implementation Based On Unfolding, Pipelining and Retiming
30	Design of an Bus Bridge between OCP and AHB Protocol (VHDL)
31	Design of Gigabit Ethernet MAC (Medium Access Control) Transmitter (VHDL)
32	Design of an AMBA-Advanced High performance Bus (AHB) Protocol IP Block (VHDL)
33	Design of Data Encryption Standard (DES) (Verilog)
34	Design of Distributed Arithmetic FIR Filter (Verilog)
35	Design of Universal Asynchronous Receiver Transmitter (UART) (VHDL)
36	Design of Triple Data Encryption Standard (TDES) (Verilog)

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37	Design of 16 Point Radix-4 FFT (Fast Fourier Transform) Algorithm (Verilog)
38	Design of Dual Elevator Controller (Verilog)
39	Design of an ATM (Automated Teller Machine) Controller (Verilog)
40	Design of 8-Bit Pico Processor (VHDL)
41	Design of JPEG Image compression standard (Verilog)
42	Design of Digital FM Receiver using PLL (Phase Locked Loop) (VHDL)
43	Design of 16-bit QPSK (Quadrature Phase Shift Keying) (Verilog)
44	Design of 16-bit QAM (Quadrature Amplitude Modulation) Modulator (Verilog)
45	Design of AES (Advanced Encryption Standard) Encryption Algorithm with 128-bits Key Length(VHDL)
46	Design of RS-232 System Controller (Same as UART) (Verilog)
47	Design of Floating-Point Multiplier using IEEE-754 Standard (Verilog)
48	Design of CRC (Cyclic Redundancy Check) Generator (Same as LFSR) (Verilog)
49	Design and Implementation of OFDM Transmitter (Same as FFT/IFFT Blocks for OFDM) (VHDL)
50	Design of 8-bit Microcontroller (VHDL)
51	An Efficient Implementation of Floating Point Multiplier
52	An On-Chip AHB Bus Tracer With Real-Time Compression and Dynamic Multi-resolution Supports for SOC.
53	Design and Characterization of Parallel Prefix Adders using FPGAs
54	Radix-8 Booth Encoded Modulo 2n-1Multipliers With Adaptive Delay for High Dynamic Range Residue Number System.
55	Reducing the Computation Time in (Short Bit-Width) Two's Complement Multipliers
56	Self-Immunity Technique to Improve Register File Integrity against Soft Errors